Department of Instrumentation and Control Engineering

End Semester Examinations January 2022

Analog Electronic Circuits – ICE 2151

PART B Question Paper

Instructions: *Answer All Questions, missing data may be suitably assumed*
Writing + Submission Time: 75 +10 minutes

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1. For the circuit shown in **Fig. Q1**, find

i. The voltage at node 'X' by viewing 'M1' as a Common Source stage degenerated by the impedance seen at the source of 'M2'.
ii. The voltage at node 'Y' by viewing 'M1' as a source follower and 'M2' as a common gate stage.
iii. The differential voltage gain $(V_X-V_Y)/Vin$

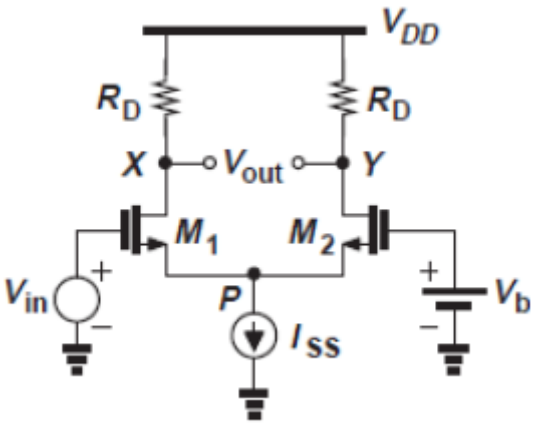

Fig. Q1 **[4M]**

2. Design a common source amplifier of **Fig. Q2** satisfying the following conditions
   i) When $\lambda = 0$, RG = 0, small signal gain is 5
   ii) When $\lambda \neq 0$, RG = 0, small signal gain is 4.88
   iii) When $\lambda = 0$, RG = 10kΩ, small signal gain is 4

   Assume V_{DD} = 1.8V, V_G = 1V, I_D = 2mA, R_S = 100Ω, V_{TH} = 0.4V, $\mu_n C_{OX}$ = 100μA/V^2. With R_G = 0, what would be the maximum gain that could be obtained from the circuit?
   iv)

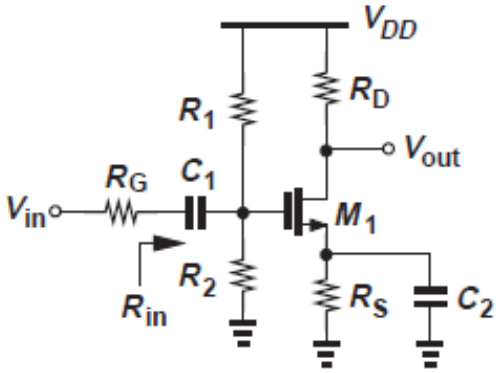

Fig. Q2

[4M]

3. Design a circuit to drive a 50Ω load with a voltage gain of 0.5 and a power budget of 10mW. Assume $\mu_n C_{ox}$ = 100 μA/V^2, V_{TH} = 0.5 V, λ = 0, and V_{DD} = 1.8 V **[3M]**
4. Consider a NMOS with W=2μm, L=0.18μm and 0.7V across its gate and source terminals. Determine it's all small signal parameters. Assume $\mu_n C_{ox}$=100μA/V^2, V_{th}=0.4V, λ=0 and V_{DD}=1.8V. **[3M]**
5. Find the loop gain and closed loop gain of the circuit shown in **Fig. Q5**. **[3M]**

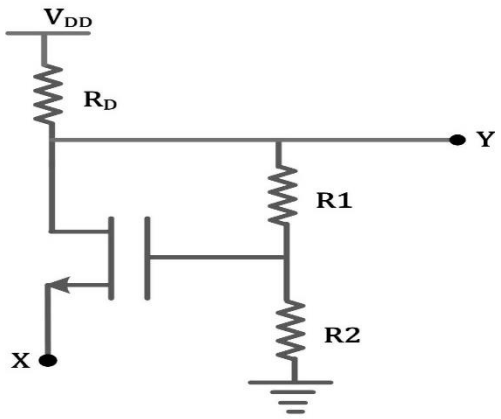

Fig. Q5

6. Calculate the oscillating frequency of a FET Hartley oscillator with C = 250pF, L_1 = L_2 = 1.5 mH, and mutual inductance between L_1 and L_2 is 0.5 mH. **[3M]**

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