END SEMESTER EXAMINATIONS (JANUARY 2022) - QUESTION PAPER - PART A

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COURSE CODE : ICE 2152
COURSE NAME : Digital Electronic Circuits
SEMESTER : III
DATE OF EXAM : 29/01/2022
DURATION : 45 + 3 minutes

Instructions for Students:
(1) ANSWER ALL THE QUESTIONS.
(2) EACH QUESTION CARRIES 1 MARK.
(3) YOU ARE INSTRUCTED TO INFORM THE INVIGILATOR AFTER SUBMISSION OF THIS FORM IN THE CHAT SECTION.

* Required

* This form will record your name, please fill your name.

1. STUDENT NAME: *

2. REGISTRATION NUMBER: *

The value must be a number

3. Which logic gate is a basic comparator?
(1 Point)

- NAND
- NOR
- X-OR
- X-NOR

4. The logic family which gives complementary output is
(1 Point)

- CMOS
- ECL
- TTL
- MOS

5. The terms which cannot be combined further in the tabular method is called
(1 Point)

- Selective prime implicants
- Essential prime implicants
- Prime implicants
- Implicants

6. The most popular and most widely used IC family is
(1 Point)

- ◯ MOS
- ◯ TTL
- ◯ CMOS
- ◯ IIL

7. An algorithmic state machine is not the same as
(1 Point)

- ◯ Combinational circuit
- ◯ Synchronous sequential circuit
- ◯ Clocked sequential circuit
- ◯ Finite state machine

8. A 32:1 mux can be designed using

(1 Point)

- ◯ Two 16:1 mux only
- ◯ Two 16:1 muxs and one two input AND gate
- ◯ Two 16:1 muxs and two two input OR gate
- ◯ Two 16:1 muxs and one two input OR gate

9. Which circuit hazards must be eliminated?
(1 Point)

- ◯ Sequential circuit
- ◯ Multiplexer
- ◯ Combinational circuit
- ◯ Decoder

10. The logic family with both logic levels negative is
(1 Point)

- ◯ MOS
- ◯ ECL
- ◯ CMOS
- ◯ TTL

11. A combinational circuit which is used to send data coming from a single source to two or more separate destinations is called
(1 Point)

- ◯ An encoder
- ◯ A decoder
- ◯ A demultiplexer
- ◯ A multiplexer

12. An ASM chart can be
(1 Point)

- Converted into a state table.
- Implemented using gates and flip flops.
- Converted as state diagram & state table and can be implemented using gates and flip flops.
- Converted into a state diagram.

13. For designing a finite state machine K-maps can be used for minimizing the
(1 Point)

- Number of flip flops.
- Excitation expressions of flip flops.
- Excitation and output logic expressions.
- Output logic expressions.

14. What conditions should be given to the asynchronous inputs of the flip flops for the operation of a Ring counter?

(1 Point)

- Clearing all the flip-flops.
- Presetting one flip-flop and clearing all others.
- Clearing one flip-flop and presetting all others.
- Presetting all the flip-flops

15. The output of a clocked sequential circuit independent of the input. The circuit is a
(1 Point)

- Moore machine
- Sequence detector
- Serial clock adder
- Mealy machine

16. Synchronous counters eliminate the delay problems encountered with asynchronous (ripple) counters because the:
(1 Point)

- Input clock pulses are applied only to the last stage.
- Input clock pulses are applied only to the first and last stages.
- Input clock pulses are not used to activate any of the counter stages.
- Input clock pulses are applied simultaneously to each stage.

17. In a 4-bit Johnson Counter, negative edge triggered J-K flip flops are used. Initial condition of the counter is 1100. What will be the output of the counter on the 5th clock pulse?

(1 Point)

- 0001
- 1100
- 0011
- 0111

18. How many select lines are contained in a multiplexer with 1024 inputs and one output?
(1 Point)

- ◯ 10
- ◯ 64
- ◯ 32
- ◯ 16

19. A binary-to-octal decoder is a
(1 Point)

- ◯ 1-line to 10-line decoder
- ◯ Any line to 1—line decoder
- ◯ A 4-line to 10-line decoder
- ◯ 3-line to 8-line decoder

20. A 6-bit synchronous counter uses flip flops with propagation delay time of 75us each. The maximum possible time required to change the state will be
(1 Point)

- ◯ 75us
- ◯ 450us
- ◯ 150us
- ◯ 300us

21. An error code 0011101 is detected at the receiver end for an even parity Hamming code. The error is in bit position
(1 Point)

- 6
- 5
- 3
- 4

22. Time delay device is the memory element of
(1 Point)

- Clocked flip flops
- Asynchronous circuits
- Unclocked flip flops
- Synchronous circuits

23. The race in which the stable state does not depend on an order is called

(1 Point)

- Critical race
- Defined race
- Non-critical race
- Identical race

24. A 4-variable logic circuit can be designed using
(1 Point)

- A 16:1 multiplexer
- An 8:1 multiplexer and one inverter
- Two 8:1 multiplexer and one 2:1 multiplexer
- Any of the above

25. Which one is the suitable to detecting the hazard in circuit?
(1 Point)

- Karnaugh map
- Boolean expression
- Logic gates
- Universal gates

26. The adder preferred for applications where circuit minimization is more important than speed is
(1 Point)

- Serial adder
- Full-adder
- Parallel adder
- Half-adder

27. A sequential circuit with 11 states will have

(1 Point)

- ◯ 6 flip flops
- ◯ 4 flip flops
- ◯ 3 flip flops
- ◯ 11 flip flops

28. The minimum number of 2-input NAND/NOR gates required to realize a half-adder is
(1 Point)

- ◯ 3
- ◯ 6
- ◯ 5
- ◯ 4

29. A demultiplexer is used to

(1 Point)

- ◯ Select data from several inputs and route it to a single output
- ◯ Perform aritmetic division
- ◯ Steer data from a single input to one of the many outputs
- ◯ Perform parity checking

30. A decision box in an ASM chart

(1 Point)

- ◯ Does not have exit paths.
- ◯ Has two exit paths.
- ◯ Has only one exit path.
- ◯ Has one entry and one exit path.

31. The group of bits 101101 is serially shifted (right-most bit first) into a 6-bit parallel output shift register with an initial state 010101. After the fifth clock pulse, the register contains _____.
(1 Point)

- ◯ 110101
- ◯ 101010
- ◯ 010101
- ◯ 011010

32. The characteristic equation of a J-K flip flop is _____.
(1 Point)

- ◯ Q(n+1) = JQn + KQn'
- ◯ Q(n+1) = J'Qn' + K Qn
- ◯ Q(n+1) = JQn' + K'Qn
- ◯ Q(n+1) = J'Qn + K'Qn