Exam Date & Time: 28-Apr-2022 (02:00 PM - 05:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

THIRD SEMESTER B.TECH END SEMESTER MAKE UP EXAMINATIONS, APRIL 2022

DIGITAL ELECTRONICS CIRCUITS [ICE 2152]

Marks: 50 **Duration: 180 mins.**

A

Answer all the questions.

Missing data may be suitably assumed

1) Define any four performance metrices of logic families. (2)

A)

B) $A_8\,A_4\,A_2\,A_1$ is an 8421 BCD input to a logic circuit whose output is a 1 when $A_8 = 0$ & $A_4 = 0$ & $A_2 = 1$, or when $A_8 = 0$ & $A_4 = 1$. Design the simplest possible logic circuit. (4)

C) Simply the Boolean function using K – Map in POS form:

$$f = \sum m(1,2,4,5,6,9,12,15) + d(10,13)$$ (4)

Implement using Universal logic.

2) Design a 1-bit magnitude comparator using basic gates. (3)

A)

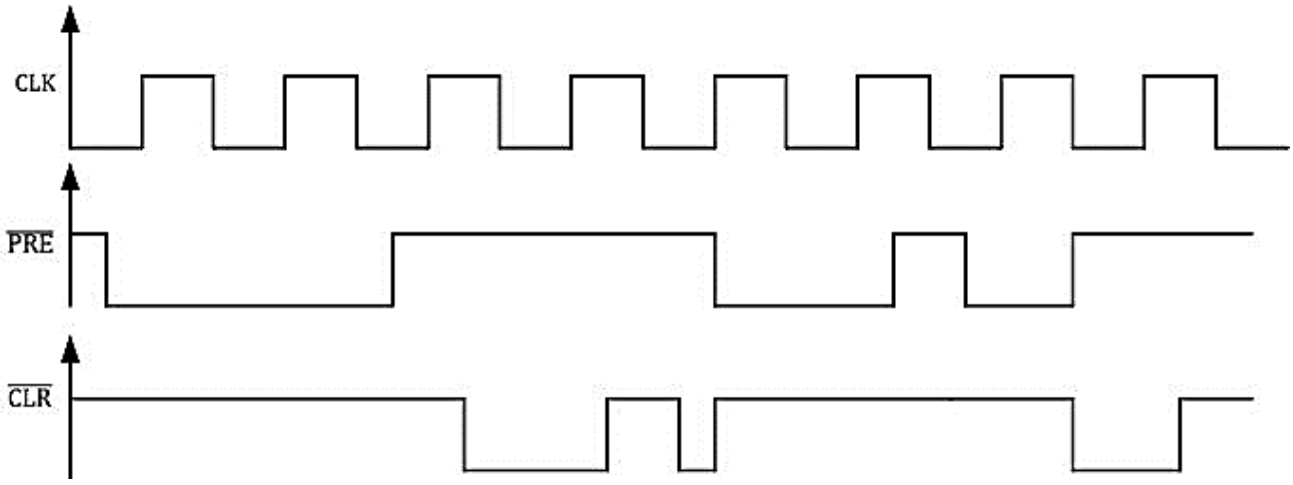
B) Implement the following logic function using a 8:1 MUX and 4:1 MUX:

$$F(A,B,C,D) = \sum m(0,3,4,7,8,10,12,15)$$ (4)

C) Design logic circuit to generate an even parity bit for a 3-bit binary input. (3)

3) The waveforms shown in the figure below are applied to a positive edge - triggered and also to a negative edge - triggered J - K flip - flop. Draw the output waveforms for both the triggering conditions assuming J = K = 1. Also assume initially output Q = 0. (2)

A)



B) Explain the working of a Ring Counter with neat logic diagram, timing diagram and the count table. (3)

C) Design a synchronous counter using D flip flops that counts 0, 1, 7, 9, 14, 0, 1, 7 .. . The unused states of the counter change to 4 at the next clock pulse. (5)

4) Design a mod 12 asynchronous counter using JK flip flops. (3)

A)

B) An asynchronous sequential circuit is described by the following excitation and output functions. (3)

$$Y = x_1\overline{x_2} + (x_1 + \overline{x_2})y$$

$$z = y$$

Draw the logic diagram of the circuit. Also derive the transition table and output map.

C) Describe the different Race conditions in Asynchronous sequential circuit with the help of suitable examples. (4)

5) A clocked sequential circuit with single input x and single output z produces an output z = 1 whenever the input x completes the sequence 101 and overlapping is allowed. Obtain the state diagram and design the circuit with D flip flops for a Moore type sequence detector. (5)

A)

B) Draw an ASM chart and state table for a 2-bit up-down counter having mode control input

M = 1: Up counting

M = 0: Down counting

The circuit should generate an output '1' whenever the count becomes minimum or maximum. (3)

C) Explain the various components used in arithmetic state machine. (2)

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