DEPARTMENT OF MECHATRONICS

III SEMESTER B. TECH MECHATRONICS

END SEM EXAM

Subject: Digital System Design **Subject Code: MTE 2152**

Time: 45 Min + 3 Min **Date: 24/1/2022**

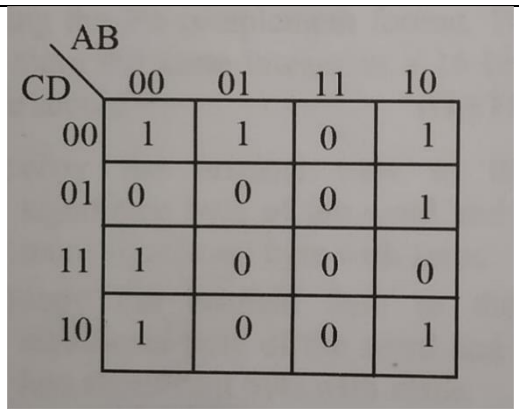
Part-A

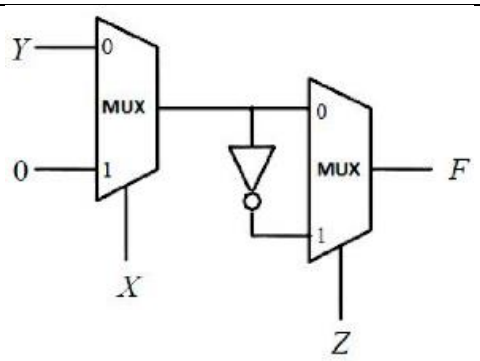
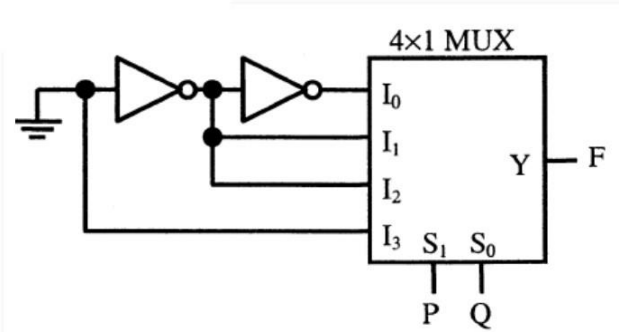
Note: All Questions carry equal mark (One mark each).

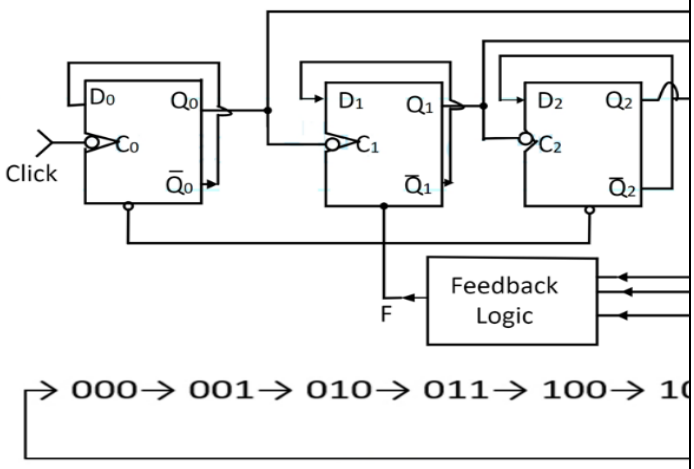
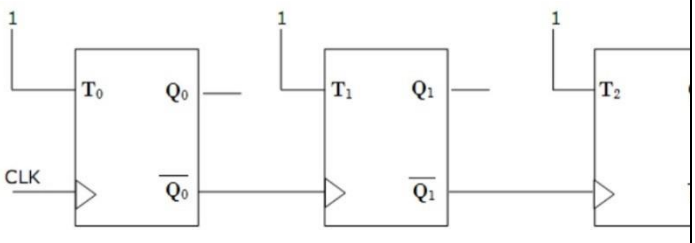
All questions are compulsory and there is No negative marking for wrong answer.

Q. No.		M	CO	PO	LO	BL
1.	Which gate is a basic logic gate? a. XOR Gate b. NOT Gate c. NAND Gate d. NOR Gate	1	1	1	1	2
2	De Morgan's Law states that a. A−+B−= AB−*A-+B-= AB-* b. c. AB−*AB-* d. = e. A−*A-* f. B*B* g. h. AB−*AB-* i. = j. A−*A-* k. + l. B*B* m. n. AB−*AB-* o. = A + B	1	1	1	1	1
3	In negative logic a. 1-high, 0-low b. 0-high, 1-low c. 1-high, 1-low d. 0-high, 0-low	1	1	1	1	1

4	Convert the binary number 1111.0010_2 to decimal. a. 115.125 b. 15.125 c. 15 d. 1.5	1	1	3	1	1
5	2's complement representation of -17 is a. 101110 b. 101111 c. 111110 d. 110001	1	2	1	1	2
6	Decimal 43 in hexadecimal and BCD number system is respectively. a. B2, 0100 0011 b. 2B, 0100 0011 c. 2B, 0011 0100 d. B2, 0100 0100	1	2	1	1	1
7.	Convert binary number (1101) into gray code: a. 1000 b. 1100 c. 1010 d. 1011	1	2	1	1	1
8.	11001, 1001 and 111001 corresponds to the 2's complement representation of which one of the following sets of numbers? a. 25, 9 and 57 respectively b. -6, -6 and -6 respectively c. -7, -7 and -7 respectively d. -25, -9 and -57 respectively	1	1	1	1	2
9.	K-map for a Boolean function is shown in figure. The number of essential prime implicants for this function is	1	1	1	1	2

	 a. 4 b. 5 c. 6 d. 81					
10.	The logic expression Y=A+A−B *Y=A+A-B* is equivalent to a. b. Y=AB *Y=AB* c. d. Y= A−B *Y= A-B* e. f. Y=A−+B *Y=A-+B* g. h. Y=A+B *Y=A+B* i.	1	1	3	1	3
11.	In half adder carry output is high if inputs are a. 0,0 b. 1,1 c. 1,0 d. 0,1	1	1	1	1	2
12.	Consider the circuit shown in the figure.	1	1	3	1	3

	 The Boolean expression F implemented by the circuit is a. [Equation] b. [Equation] c. [Equation] d. [Equation]					
13.	Without any additional circuitry, an 8:1 MUX can be used to obtain a. Some but not all Boolean functions of 3 variables b. All functions of 3 variables but none of 4 variables c. All functions of 3 variables and some but not all of 4 variables d. All functions of 4 variables	1	2	1	1	2
14.	The logic function implemented by the circuit below is (ground implies a logic'0')  a. [Equation] b. [Equation] c. [Equation] d. [Equation]	1	2	1	1	3
15.	A master slave flip-flop has the characteristic that a. change in the input immediately reflected in the output	1	3	2	2	2

	b. change in the output occurs when the state of the master is affected c. change in the output occurs when the state of the slave is affected d. both the master and slave states are affected at the same time					
16.	A ripple counter using negative edge-triggered D-flip flops is shown in Figure. The flip-flops are cleared to '0' by a '0' at the R input. The feedback logic is to be designed to obtain the count sequence shown in the same figure.  The correct feedback logic is: a. [Equation] b. [Equation] c. [Equation] d. [Equation]	1	3	4	1	1
17.	The given figure shows a ripple counter using positive edge triggered flip-flops. If the present state of counter is $Q_2Q_1Q_0 = 011$, then its next state ($Q_2Q_1Q_0$) will be  a. 010 b. 100	1	3	2	1	1

	c. 111 d. 101					
18.	Unused states are treated as Don't cares conditions during the a. Design of a circuit b. Execution c. Pulse trigger d. Edge trigger	1	1	1	1	1
19.	Memory elements in clocked sequential circuits are called a. Latches b. Flip-flop c. Signals d. Gates	1	2	1	1	1
20.	A counter that flows the binary sequence is called e. Ripple counter f. Edge counter g. Binary counter h. Level counter	1	3	3	2	1
21.	Which of the follwing is not a sequential circuit? a. Flip-flop b. Counter c. Shift register d. Multiplexer	1	3	2	1	1
22.	The negative transition in flip-flops are reffered to as a. Clock b. Negative edge c. Positive edge d. Pulse transition	1	3	2	1	1
23.	The full form of PIPO is _____ a. Parallel-in Peripheral-out b. Parallel-in Parallel-out c. Peripheral-in Parallel-out d. Peripheral -In Peripheral-Out	1	3	2	1	1

24.	How many test patterns are required to test the circuit using counters? a. 2^n b. $2^{(n-1)}$ c. $2^n - 1$ d. $2^n + 1$	1	3	2	1	1
25.	What happens if the input is low in FSM? a. Change of state b. No Transition in state c. Remain in a single state d. Invalid state	1	3	2	1	1
26.	In the FSM Diagram, what does arrow between the circles are represent? a. Change of state b. State c. Output value d. Initial state	1	3	2	1	1
27.	FPGA stands for a. Field Program Gate Array b. First Program Gate Array c. Field Programmable Gate Array d. First Programmable Gate Array	1	3	2	1	1
28.	Many companies are transitioning to using FPGAs for their processor designs instead of ASICs. Why? a. FPGAs always outperform an ASIC. b. The development cycle of the FPGA is much shorter. c. FPGAs are more space-efficient. d. FPGAs are both smaller and faster. e. None of the above.	1	4	1	1	1
29.	Most FPGA logic modules utilize a(n) _____ approach to create the desired logic functions. a. AND array b. Look-up table c. OR array d. AND and OR array	1	4	1	1	1

30.	In spartan-3 family architecture, which programmable functional element accepts two 18-bit binary numbers as inputs and computes the product? a. Configurable Logic Blocks b. Input Output Blocks c. Block RAM d. Multiplier Blocks	1	4	1	1	1

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

DEPARTMENT OF MECHATRONICS ENGINEERING
III SEMESTER B. TECH (MECHATRONICS ENGINEERING)

END SEMESTER EXAMINATIONS PART B, JAN 2022

SUBJECT: DIGITAL SYSTEM DESIGN [MTE 2152]

Time: 75 Min + 10 Min **Date: 24/1/2022**
Max. Marks: 20

Q. No.		M	CO	PO	LO	BL
1A	Solve the given equation using VEM, to obtain the minimum SOP expression. $F(A,B,C,D,E) = \sum m(1,4,8,11,12,14,15,24,25,30) + d(6,9,13,16,17,22,23,28,29)$	**5**	**CO1**	PO1, PO3, PO12	1, 7, 13	2,3
1B	Design a 4-bit 4 state ring counter with a single circulating '0' using 74194	**3**	**CO3**	PO1, PO2, PO3, PO12	3,7, 8,9, 13	2,3
1C	Develop a MOD 14 counter using 7493 IC.	**2**	**CO3**	PO1, PO2, PO3, PO12	3,7, 8,13 ,18	2,3
2A	Illustrate the dataflow Verilog code for a single bit full adder. Using this as a component, develop a Verilog code for a 4-bit full adder.	**4**	**CO5**	PO1, PO5, PO12	3,6, 8,9, 13	2,3
2B	Demonstrate a 4 to 16 decoder, using 3 to 8 decoders.	**3**	**CO2**	PO1, PO2, PO3, PO12	2, 7, 9, 13	2,3
2C	Construct a JK flip flop using D flip flop	**3**	**CO3**	PO1, PO2, PO3, PO12	3,7, 8,9, 13	2,3