MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

FIFTH SEMESTER B. TECH (ELECTRONICS AND INSTRUMENTATION)

PROCTORED ONLINE END SEMESTER EXAMINATION Dec. 21/Jan. 22

SUBJECT: **MICROCONTROLLERS (ICE 3152)**

TIME: 45 minutes **DATE: 28-12-2021** **MAX.MARKS:30**

PART A

1. Using Timer 1 in mode 1, the 8051 needs to generate a frequency of 100 KHz using a clock of 22 MHz. The value to be loaded into the timer registers are:
    a. FFE7H
    b. FFEFH
    c. FFF7H
    d. FFFEH

2. What is the time delay generated by the subroutine below. FFF2H is the value loaded in the timer register. Assume XTAL is 11.0592 MHZ.
   Delay: SETB TR0
   Again: JNB TF0, AGAIN
   CLR TR0
   CLR TF0
   RET
    a. 38.30 us
    b. 30.38 us
    c. 15.19 us
    d. 27.45 us
3. In the instruction MOV TH1, #-200, find the hex value for the TH1 register.
    a. -38
    b. 38H
    c. -38H
    d. 38
4. While connecting the 8051 to the RS232, the MAX232 chip is used as a
    a. Current sink
    b. Voltage stabilizer
    c. Line driver
    d. Serializer

5. If TH1 = FCH to obtain a baud rate of 9600, XTAL1 is
    a. 16MHZ
    b. 22MHZ
    c. 11.0592MHZ
    d. None of the above
6. With SMOD = 1, and crystal frequency is 22MHz, the baud rate obtained for TH1 = -3 is
    a. 19,093
    b. 38,186
    c. 9600
    d. 4800
7. The instruction to enable the interrupt to transmit serial data is _____
    a. MOV IE, #10001000
    b. MOV IE, #10010000
    c. MOV IE, #0010000
    d. MOV IE, #0110000
8. The instruction used to bypass the memory space allocated to the IVR is
    a. SJMP MAIN
    b. CLR IVR
    c. SETB IVR
    d. LJMP MAIN
9. As per the data sheet of the 8051, for successful latching of the INT0, the pin must be held low until
    a. The execution of RETI instruction
    b. For one machine cycle
    c. Till ISR starts to execute
    d. Throughout the execution of the program
10. On power-up, the 8051 uses which RAM locations for R0-R7
    a. 00 – 0FH
    b. 00 – 07H
    c. 00 – 7FH
    d. 00 – 2FH

11. When data is pushed onto the stack, the stack pointer
    a. Increments
    b. Decrements
    c. Depends on the configuration
    d. None of the above

12. The number of user-accessible 16-bit registers in the 8051 are:
    a. 1
    b. 2
    c. 3
    d. 0
13. On power-up, _____ is loaded with 00H
    a. PSW
    b. SP
    c. PC
    d. ISR
14. When there is an overflow due to an arithmetic operation, then the bits of which register are affected
    a. SP
    b. DPTR
    c. PSW
    d. PC
15. Program counter stores what:
    a. Data of the instruction to be executed
    b. Address of the instruction to be executed
    c. Data of the previous instructions
    d. Address of the previous instruction
16. What is the address of the SFRs?
    a. 00h to FFh
    b. 80h to FEh
    c. 80h to FFh
    d. 70h to 80h
17. Who provides the clock source to the 8051 timers, if 6th bit of TMOD is 1?
    a. Crystal Oscillator
    b. External clock source
    c. Machine cycle
    d. User configurable

18. Find a number that, when XORed to the A register, results in the number 3Fh in A.

MOV R0, A

XOR A, #3Fh

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    a. XOR A, R0

b. XOR R0, A
c. MOV A, R0
d. MOV R0, A

19. Which of the following instruction is not correct
    a. JMP @A+DPTR
    b. ACALL LOOP
    c. JNB P1.3, LOOP
    d. JMP @A+PC
20. Which of the following is true
    a. The operation of RETI is to POP two bytes from the stack into the PC and reset the interrupt enable flip-flops.
    b. The operation of RETI is to POP two bytes from the stack into the PC and set the interrupt enable flip-flops.
    c. The operation of RETI is to POP three bytes from the stack into the PC and reset the interrupt enable flip-flops.
    d. The operation of RETI is to POP three bytes from the stack into the PC and set the interrupt enable flip-flops.
21. By using _____ instruction no flags of PSW are affected?
    a. ORL A, #20h
    b. PUSH DPL
    c. RR A
    d. All the given
22. Which of the following is correct
    a. ORL instruction is used to mask the status of the bits
    b. ORL C, /b alter the addressed bit b
    c. INC instructions that operates on the port direct address alter the latch for that port
    d. All the given
23. The value sent to the DAC (in decimal) for an angle 90 degree, while generating the sine wave is
    a. 255
    b. 128
    c. 192
    d. 0
24. Which of the following is true
    a. By modulating the width of the pulse applied to DC motor, we can increase or decrease the motor speed.
    b. Reset is a non-maskable active high interrupt line
    c. 8051 does not have dedicated internal hardware for PWM generation
    d. All the given

25. When 4*4 keyboard matrix is connected to 8051, which of the following correct step sequences are used to detect the key that is being pressed.

i) Check whether key is pressed or not

ii) Masking of bits

iii) Ensure all keys are released initially

a. i) iii) ii)
b. ii) i) iii)
c. iii) ii) i)
d. ii) iii) i)

26. Calculate the execution time for the following subroutine (assume time period for 1 machine cycle is 2 microsec)

Instruction	No.of machine cycle
MOV R3,#04H	1
LOOP3:MOV R2, #0F5H	1
LOOP2:MOV R1, #0FFH	1
LOOP1:DJNZ R1, LOOP1	2
DJNZ R2, LOOP2	2
DJNZ R3, LOOP3	2
RET	2

a. 1 second
b. 1.5 second
c. 2 second
d. 0.5 second

27. Which of the following is not true in case of 8051

a. JB and JNB cannot be used for any bits of I/O ports 0, 1, 2, and 3
b. ANL can be used to read the content of an internal port latch
c. Using the instruction JNB P1.5, LOOP assumes that bit P1.5 is an input
d. All the given

28. Which of the following is true for ARM

a. A code area is usually read-only area
b. The program written in ARM assembly language can be assembled in a PC with different processor
c. Thumb instructions are either 16 or 32 bits long
d. All the given

29. Which of the following is not true for ARM

a. In FIQ mode R8-R14 are replaced by another set of registers which are suffixed by FIQ
b. Having register R13, helps to reduce the delay associated with call and interrupt
c. ARM has 37 registers each of which is 32 bits long
d. Most of the tasks run under unprivileged mode of ARM

30. Which of the following is true for ARM

a. SPSR is available for all the operating modes of ARM
b. Besides exceptions, processors can also be interrupted by instructions
c. ARM has 107 general purpose registers
d. All the given

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TIME: 75 minutes **DATE: 28-12-2021** **MAX.MARKS:20**

Note: Answer All questions.

1	A	With a neat diagram bring out the differences between Von Neumann and Harvard Architecture.	2
	B	Write a program with a delay subroutine to generate a square wave of 25% duty cycle on bit 3 of port 1.	3
	C	Write an 8051 ALP to control the stepper motor, by assuming code sequence is stored in a memory location pointed by DPTR. Use suitable delay routine and comment on each of instructions used. Also draw interfacing diagram.	5
2	A	Generate a square wave of 75% duty cycle at the pin no. 9 of LPC 2148 Port0.	2
	B	Discuss the PWM unit of LPC2148 with block diagram.	3
	C	With neat diagram explain AMBA and MAU of ARM.	5

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Scheme of valuation

Q.No	Scheme	Marks
1A		
1B		
1C	Interfacing circuit using ULN 2003 Use of sequence1000,0100,0010,0001 or any other Use MOVC A,@A+DPTR to access the LUT Program+ Comments	1M 1M 1M 1M+1M
2A	IO0DIR=0XFFFFFFFF IO0SET=0X003C0000 IO0CLR=0X003C0000	1M

	Program with delay	1M
2B	Block diagram with Timer Control register, timer count register, prescalar, match register, match control Explanation	1M 2M
2C	User, FIQ, IRQ, Supervisor, Abort, Undef, System with explanation Block diagram of register set of ARM	3.5M 1.5M

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