Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SEVENTH SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION
DECEMBER 2021-JANUARY 2022
SUBJECT: ANALOG AND MIXED SIGNAL DESIGN (ECE -4061)

TIME: 75 MINUTES **MAX. MARKS: 20**

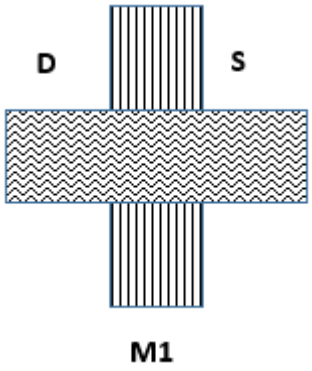
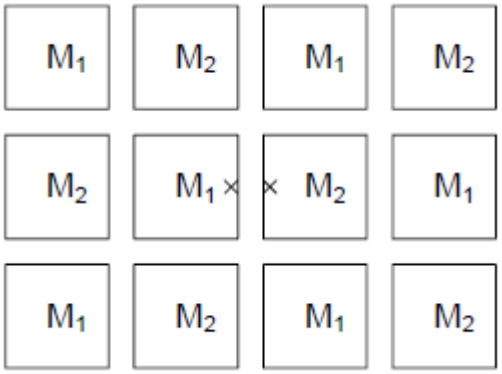
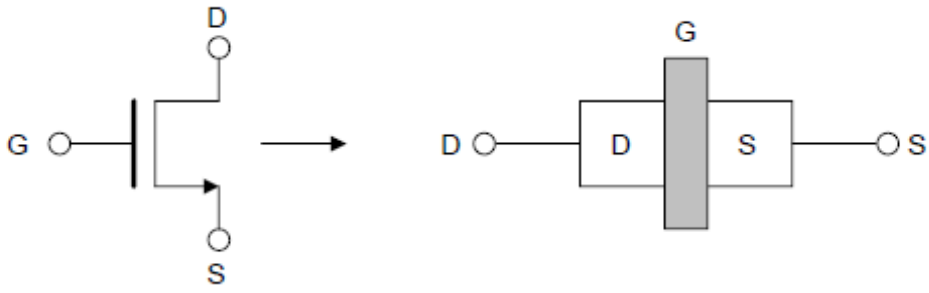
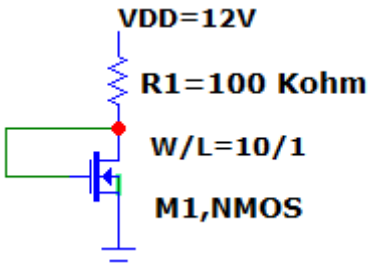
Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

Q. No.	Questions	M
1A.	Construct the small signal model of basic Wilson current mirror. How the error/variation in the current ratio (Iout/Iref) is rectified in the modified version of Wilson current mirror?	4
1B.	Explain the working of 3-bit SAR ADC to convert analog voltage of 0.7 V to digital value with neat diagram.	3
1C.	Construct the small-signal model of the PMOS transistor with CLM and Body effect. Calculate the values of the gm (transconductance), gmbs/gmb (backgate transconductance) and gds (output conductance) for n-channel device if I_D=50 µA , Vsb=2V, η=0.1 and W/L=1/1. MOS parameters are illustrated in **Table 1.**	3
2A	(i) In a typical MOS fabrication process, M1 transistor has been fabricated as shown in Fig. 2A (i). Vendor want to fabricate another transistor side by side so that current from both the transistor should flow in same direction. Propose a scheme to achieve this. (ii) On a wafer, multiple devices have fabricated as shown in Fig.2A(ii) by the vendor without considering the variations of processing environment. This leads to changes in electrical properties affecting the performance of circuits. Propose a scheme by redrawing the device layouts to increase the performance and name the mechanisms.	5

Parameters	Values
V_T	0.7 V
K', transconductance parameter	110 µA/V^2
ϒ, bulk threshold parameter	0.4 $V^{1/2}$
λ CLM parameter	0.04 V^{-1}
$2\|\varphi_F\|$	0.7 V

Table. 1

	(iii) Vendor has fabricated the wide MOS transistor as shown in Fig.2A(iii). In order to decreases parasitic capacitance and resistance, propose a scheme to achieve this.  **Fig.2A (i)**  **Fig.2A (ii)**  **Fig.2A (iii)**	
2B.	(i) Calculate the drain current for the transistor in **Fig.2B** if $\lambda = 0$. (ii) Repeat if $\lambda = 0.025\ V^{-1}$. (iii) Repeat part (i) if the W/L ratio is changed to 25/1. Vtn=0.75 V. $\beta n=100\ \mu A/V^2$.  **FIG.2B.**	3
2C.	Design a 3-bit current steering DAC. Assume I= 1 μA, R= 1 MΩ.	2