Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

VII SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION

DECEMBER 2021-JANUARY 2022

SUBJECT: Digital Design Verification (ECE - 4062)

TIME: 75 min **MAX. MARKS: 20**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. For the state machine given in **TABLE Q1A**, discover the equivalence partitions and write corresponding reduced state machine. PS, NS, X, and Z represent present state, next state, input, and output respectively. **4**

TABLE Q1A

PS	NS, Z	
	X=0	X=1
A	B,0	E,0
B	E,0	D,0
C	D,1	A,0
D	C,1	E,0
E	B,0	D,0

1B. Illustrate that the circuit shown in **Fig Q1 B** is equivalent to 1-bit full adder using equivalence checking. **3**

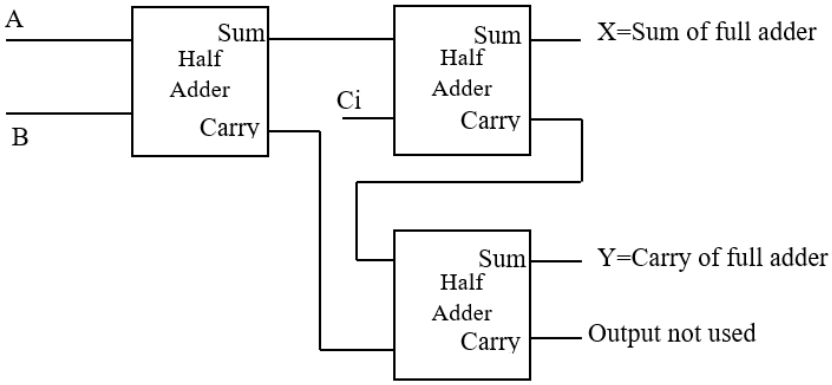

Fig Q1 B

1C. Explain the challenges involved in verifying a 64-bit counter. Assume that simulation tool used for verification can verify 1000000 transition per second. **3**

2A. Write a System Verilog class for generating the random input values for 4 to 1 multiplexer and display the result in the given form **4**

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 Generator
 d=1010, s=0
 f=x
----------------------------------------
```

Note: values of inputs d and s may be different due to randomization

2B.	Write a SystemVerilog class to communicate the values of d and s from generator class (Q.2A) to the driver class.	3
2C.	Discuss the corner case with an example.	3