Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FOURTH SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION

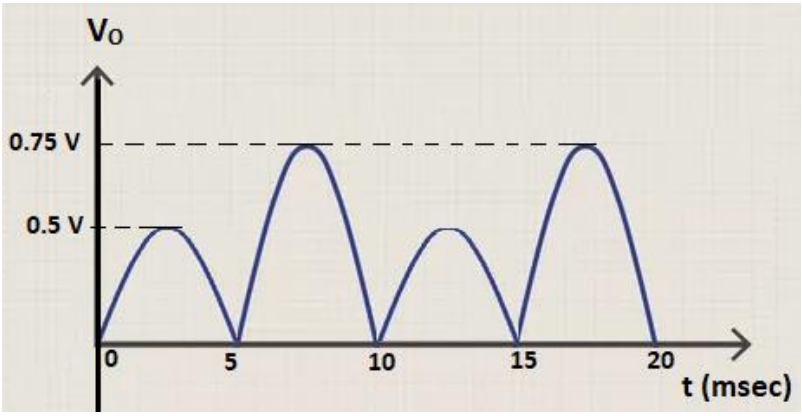
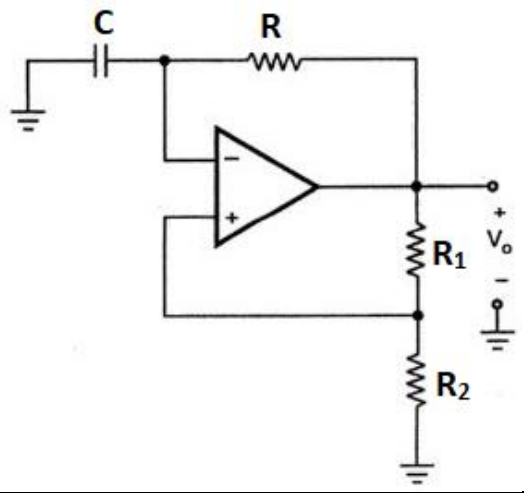
JUNE 2022

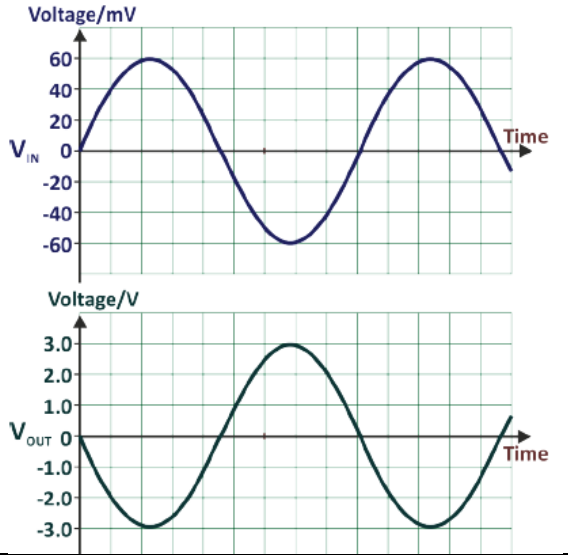
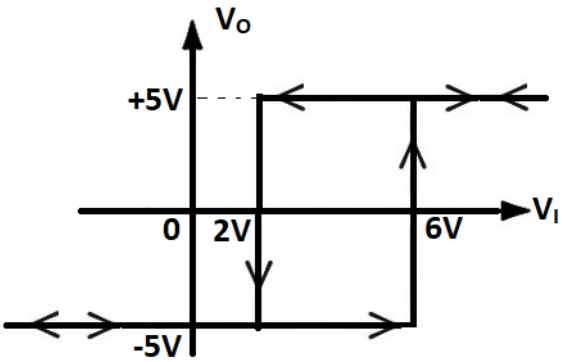
SUBJECT: LINEAR INTEGRATED CIRCUITS (ECE - 2253)

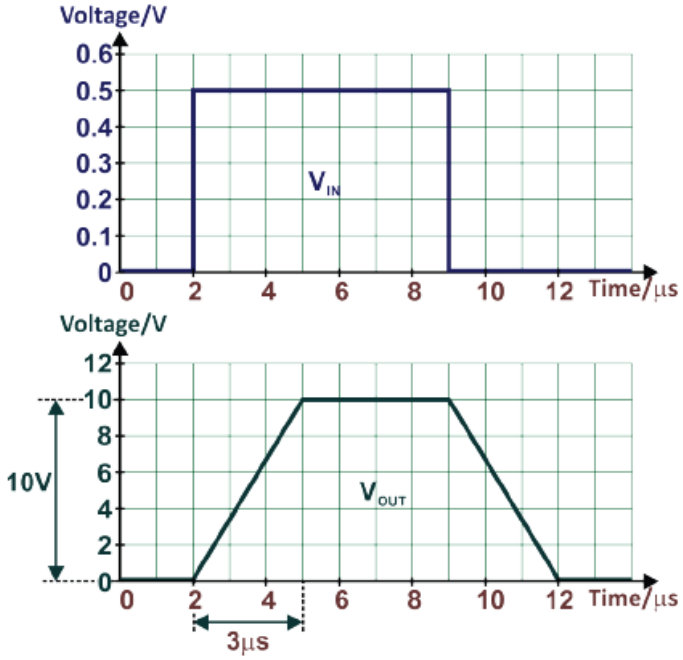
TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

Q. No.	Questions	M*	C*	A*	B*
1A.	The input signal to a circuit is $V_{in} = 0.5\sin(100\pi t)$ volts. Design a circuit using two OPAMP to obtain the output as shown in Figure. Also using suitable analysis show that the circuit works as per the requirement. 	5	3		4
1B.	An OPAMP is configured for astable multivibrator operation as shown in figure. The ratio R1/R2 can be adjusted from 1.8 to 9. Calculate the output signal frequency range if the time constant RC=1msec. 	3	3		5

1C.	Draw the circuit diagram for an amplifier using OPAMP which would generate this response to the input signal shown in figure. Determine suitable values for all resistors used in the circuit. 	2	1		3
2A.	Design an OPAMP based circuit to obtain a transfer characteristic as shown in figure below. Assume power supply of ±12 volts. Derive the design equation. 	5	3		4
2B.	Suggest a suitable circuit using OPAMP to deliver a current to a variable load resistor, one end of which is grounded. The current through the load is a linear function of the source voltage and is independent of the load resistor. Also make sure that the load current is not directly drawn from the source. Derive the necessary expression.	3	1		3
2C.	The figure below shows how an amplifier output responds to a step input signal. i. Estimate the slew rate for the amplifier. ii. Calculate the maximum signal frequency that will produce distortion-free output for a sinusoidal output of amplitude 10 V.	2	1		3

					
3A.	Design a summing amplifier using single OPAMP to give the output voltage: $V_O = -2V_a + 2.5V_b + 1.5V_c$. Use feedback resistor of 2KΩ.	5	1		4
3B.	Design a FSK modulator using 555 IC which produces the frequency f1=90KHz for transmitting bit 1 and f2 =120KHz for the bit 0	3	4		3
3C.	Design a circuit to produce a pulse width of 30ms using IC 555 with Vcc =5V upon the application of negative edge trigger pulse.	2	4		3
4A.	Design a second order RC narrow band pass filter for the following specification: Mid band voltage gain = 34dB, Quality factor =10, Band width =16Hz. Also draw the gain frequency plot with all necessary values.	5	2		4
4B.	Define the following terms i) Free running frequency ii) Lock range iii) capture range.	3	4		2
4C.	Design a circuit which provides a phase shift of -90° for the sinusoidal signal of frequency 1KHz. Assume C= 0.01μF.	2	2		3
5A.	Design a circuit using 555 IC to generate a clock of 1KHz with duty cycle 60%. Modify the circuit designed to obtain a clock 1KHz with 40% duty cycle. Choose the capacitor of 0.01μF. Explain the circuit operation.	5	4		4
5B.	Design 4-Bit binary weighted resistor type DAC for the following specification. Full scale output voltage is -7.5V. The maximum current supplied by the DAC is limited to 3.75mA. Logic level 1=+5V and logic 0 = 0V. Determine the output when the input is i) 0101 ii) 1010	3	5		3

5C.	Derive the 8 bit digital output equivalent to an analog voltage of 5V for the dual slope ADC which has a maximum integrator output of -6v when the input voltage is 10V.	2	5		3

M*--Marks, C*--CLO, A*--AHEP LO, B* Blooms Taxonomy Level