Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FOURTH SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION

JUNE 2022

SUBJECT: VLSI DESIGN (ECE - 2254)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.
- Graph sheet will be provided

Q. No.	Questions	M*	C*	A*	B*
1A.	Describe the steps involved in the fabrication of CMOS inverter using SOI (Silicon on Insulator) process with neat diagram.	4	3	1	2
1B.	Implement the given words using NOR ROM and draw its stick diagram. $\begin{bmatrix} w0 \\ w1 \\ w2 \\ w3 \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 1 \\ 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix}$	3	2	1	3
1C.	Implement the given expression using pseudo NMOS logic and indicate L: W ratio of each transistor $Z = \overline{A.B + C.(D + E)}$	3	2	1	3
2A.	Describe latch-up problem in CMOS and suggest solutions.	4	3	1	2
2B.	Implement a full adder using NMOS pass transistors. Assume input and its complements are available.	3	2	1,1 2	3
2C.	Implement 3-input NOR gate using BiCMOS logic.	3	2	1	3
3A.	Describe the fabrication of N-channel Enhancement MOSFET with the help of neat diagram.	4	3	1	2
3B.	Implement full subtractor using NMOS PLA	3	5	1	3
3C.	Describe the fabrication of Depletion MESFET with the help of neat diagram.	3	5	1	2
4A.	Draw the layout of Pseudo NMOS inverter using λ based design rule.	4	4	1,1 2	3
4B.	Perform following function using ALU unit i. 1000 SUB 1001 ii. 1010 XOR 0011 iii. 0101 AND 1100	3	5	1	2
4C.	Describe the working of 4×4 barrel shifter with the help of a suitable circuit / diagram.	3	5	1	2

5A.	Find the optimal number of NMOS inverters to be cascaded so as to drive load capacitance of 0.54 pF off-chip capacitive load such that the total delay is minimized. Given that 1□Cg = 0.01pF. Give the cascaded structure with L:W ratios indicated. Find the overall delay.	4	4	1,2	2
5B.	Describe the working of bus arbitration logic using structured approach.	3	5	1	2
5C.	Describe the working of 3-T DRAM with the help of circuit and timing diagram.	3	2	1	2

M*--Marks, C*--CLO, A*--AHEP LO, B* Blooms Taxonomy Level