Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FOURTH SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION

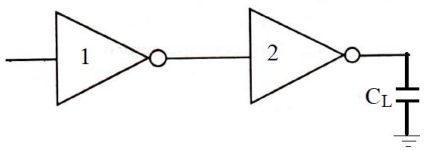
JUNE 2022

SUBJECT: VLSI DESIGN (ECE - 2254)

TIME: 3 HOURS **MAX. MARKS:50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.
- Graph sheet will be provided

Q. No.	Questions	M*	C*	A*	B*
1A.	Two Pseudo NMOS inverters are cascaded to drive a capacitive load of $C_L = 16 \square C_g$ as shown in the **Fig. Q 1A.** Calculate the pair delay in terms of τ for the inverter geometry indicated in the figure.  Inverter-1: $L_{PU}=6\lambda$, $W_{PU}=2\lambda$, $L_{PD}=2\lambda$, $W_{PD}=2\lambda$ Inverter-2: $L_{PU}=12\lambda$, $W_{PU}=4\lambda$, $L_{PD}=4\lambda$, $W_{PD}=4\lambda$ **Fig. Q1A**	4	4	1,2	3
1B.	Implement 3-input NAND gate using BiCMOS logic.	3	2	1	3
1C.	Describe the working of 4×4 cross bar switch with the help of neat diagram and list its disadvantages.	3	5	1	2
2A.	Draw the layout of depletion load NMOS inverter using λ based design rule.	4	4	1,12	2
2B.	Show that a full adder block can be used as subsystem to implement the following functions i. 2 input XNOR ii. 2 input OR iii. 2 input AND	3	5	1,12	2
2C.	Describe the working of n-bit parity generator using structured approach.	3	5	1	1
3A.	Describe the fabrication of P-channel Enhancement MOSFET with the help of neat diagram.	4	3	1	1

3B.	Explain the working on non-inverting super buffer.	3	2	1	1
3C.	Implement $Z = \overline{(A.B + C).D}$ using CMOS logic.	3	2	1	3
4A.	Describe the problem associated with N-Well CMOS process and its solution.	4	3	1	1
4B.	Describe the fabrication of Enhancement MESFET with the help of neat diagram.	3	5	1	1
4C.	Describe the working (Read and Write operation) of 6-T SRAM.	3	2	1	1
5A.	Give the circuit implementation of following multiple output function using Pseudo-NMOS PLA. F=AB+A'B'C G= A XOR B H=AB+BC+AC	4	5	1	3
5B.	Implement the given words using NAND ROM and draw its stick diagram. $\begin{bmatrix} w0 \\ w1 \\ w2 \\ w3 \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 1 \\ 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix}$	3	2	1	3
5C.	Implement N-Input NOR gate using dynamic CMOS logic.	3	2	1	3

M*--Marks, C*--CLO, A*--AHEP LO, B* Blooms Taxonomy Level