Exam Date & Time: 16-Jun-2022 (02:00 PM - 05:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

FOURTH SEMESTER B.TECH END SEMESTER EXAMINATIONS, JUNE 2022

DIGITAL SYSTEM DESIGN [BME 2253]

Marks: 50 **Duration: 180 mins.**

A

Answer all the questions.

Instructions to Candidates:
Answer ALL questions Missing data may be suitably assumed

1) Classify the Semi-custom Application Specific Integrated Circuit (ASIC). Identify the one such device with programmable provision and discuss its benefit over full-custom ASIC. (3)

A)

B) Design a three input CMOS AND gate with a neat circuit, mention the details of pullup and pull-down transistors. Verify the operation of gate considering possible input combinations (3)

C) Design latch using TG and other basic gates. Explain its operation. (4)

2) State Shannon's expansion theorem. Design a MUX based circuit by applying the theorem to find the co factors of the following function with respect to variable w1: (4)

A) f (w1,w2,w3) = w1w2+w1w3+w2w3.

B) Design an AND-OR plane of a PLA considering NMOS programmable switches to realize the following function: Y= A'B +C'D. Draw the diagram and explain the operation of the given planes. (3)

C) Explain the architecture of Complex PLD with a central PIA. Differentiate how Complex PLD is different from a Simple PLD. (3)

3) Apply the knowledge of the NMOS transistor and arrange them as SRAM cell circuit, and illustrate the working details of the circuit. (3)

A)

B) Design a Verilog HDL module for realizing the following function using gate primitive: F= AB+A'C+CD. Show that instance of the specified module are created in two styles. Note: Write comments on each line. (3)

C) Identify the benefit of Programmable Logic devices. Draw the architecture of a simple Programmable array logic and explain how the macrocell helps in the design of a sequential or combinational logic circuit. (4)

4) Describe the general architecture of FPGA. Further elaborate the elements configurable logic block (CLB) and discuss its role in the design of a digital system. (4)

A)

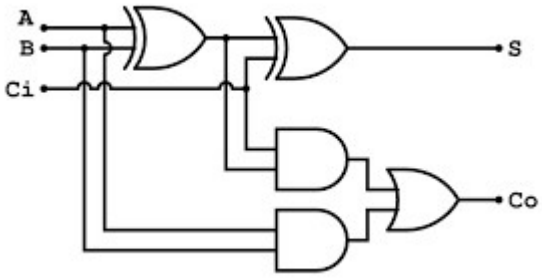
B) Design 2 input LUTs design, for realising the given function, F= A'B+ CD. Write the details of function table and the LUT used for each stage. (3)

C) Identify the general important steps considered during the design a system using FPGA. Illustrate the role of HDL in the digital system design are using FPGA. (3)

5) Design a Verilog HDL module to synthesis a half adder circuit using assignment statements. Consider a time scale of 1ns/ 1ps. (3)

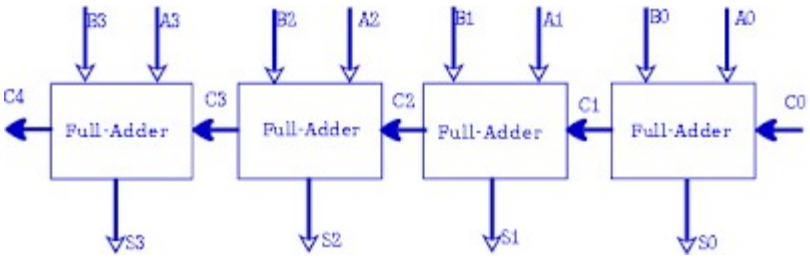
A)

B) Design a Verilog module for 1-bit full adder (as shown in figure 5(i). Write a new Verilog module for synthesising a 4-bit adder described in the figure 5(ii), using the instances of the above designed 1-bit adder module. Specify the instantiation method used.



(4)

5 (i) 1 bit adder logic circuit



5 (ii) 4bit adder circuit

C) Design a basic sequential circuit module using Verilog HDL module using always block. (3)

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