Exam Date & Time: 18-Jun-2022 (09:00 AM - 12:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

FOURTH SEMESTER B.TECH END SEMESTER EXAMINATIONS, JUNE 2022

DIGITAL SYSTEM DESIGN [ICE 2251]

Marks: 50 **Duration: 180 mins.**

A

Answer all the questions.

1) Explain different types of verilog modeling styles with examples. (6)

A)

B) Develop structural code for 4:1 multiplexer. (4)

2) Write behavioural verilog code for 4 bit upcounter. Explain how the counter output divides the clock using a timing diagram. (6)

A)

B) Develop dataflow verilog code for a binary to octal decoder. (4)

3) Show how PLA circuit can be programmed to implement 3-bit binary to grey code convertor. (3)

A)

B) What are the difference between tasks and functions? (3)

C) Implement Moore machine to detect the overlapping sequence 1110. (4)

4) Explain the general structure of a CPLD. Write any two application of CPLDs & FPGAs. (3)

A)

B) Explain event based timing control with examples. (3)

C) Write a verilog code that outputs a pulse with ON period of 50ms and OFF period of 25ms. Assume input clockperiod of 10ms. (4)

5) Explain the programming technologies used to make the FPGAs field programmable. (3)

A)

B) What are different types of structured procedures in verilog? Explain with use cases. (3)

C) Draw the block diagram and explain each of the blocks of a mealy machine. (4)

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