Exam Date & Time: 11-Jun-2022 (09:00 AM - 12:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

DEPARTMENT OF ICE
FOURTH SEMESTER B.TECH END SEMESTER EXAMINATIONS, JUNE 2022

LINEAR INTEGRATED CIRCUITS [ICE 2254]

Marks: 50 **Duration: 180 mins.**

A

Answer all the questions.

Instructions to Candidates: Answer ALL questions Missing data may be suitably assumed. Symbols have their usual significance.

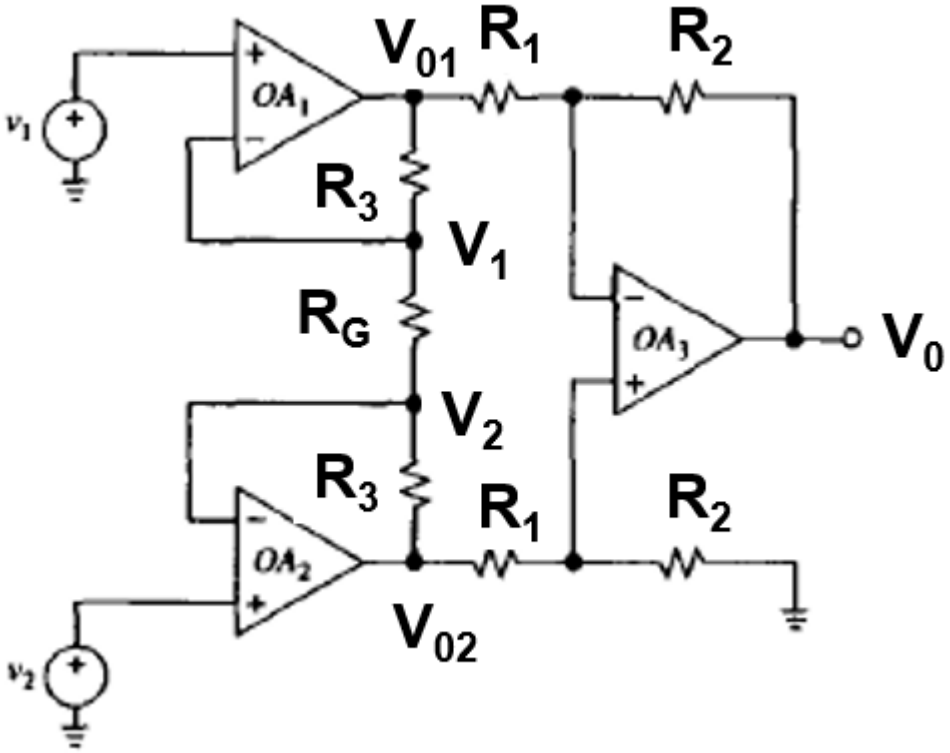
1) A) An inverting amplifier with $R_1 = 15k\Omega$, $R_2 = 22k\Omega$ (feedback resistance) and $V_i = 3.3V$ drives a $2.5k\Omega$ load. Assuming $\pm 12V$ supplies and $I_Q = 0.5mA$, find i_{CC}, i_{EE} and i_o. Find the power dissipation inside the op-amp. (4)

B) Explain the working of floating load voltage-current (V-I) converter with suitable circuit diagram and write the expression of voltage compliance in both inverting and non-inverting configurations. (4)

C) Design a multiple feedback band pass filter with $f_o = 2.8kHz$, $Q = 10$, $H_o = 30dB$. Consider $C_1 = C_2 = 0.47\mu F$. (2)

2) A) Explain the different compensation techniques used for nullifying the input offset in operational amplifiers. (4)

B) Determine the output voltage for the circuit shown. Given: $R_3 = 20k\Omega$, $R_G = 200\Omega$, $R_1 = 20k\Omega$, $R_2 = 40k\Omega$, $V_1 = 8.995V$ and $V_2 = 9V$. (4)



C) An op-amp based astable multivibrator circuits constructed using the following components, R_1 = 25 kΩ, R_2 = 25 kΩ, R = 45 kΩ and C = 0.01 μF and powered with V_{CC} = 15V, V_{EE} = -15V. Calculate the frequency of oscillation of the circuit. (2)

3) With suitable circuit diagram, explain the working of any one application of comparator. (3)

A)

B) Describe working of full-wave precision rectifier using suitable circuit diagrams. (3)

C) Explain operation of a monostable multivibrator using op-amp with help of a circuit diagram. Also draw its timing diagrams. (4)

4) Design an astable multivibrator using 555 timer with duty cycle of 83% and frequency of 1.8kHz. (3)

A)

B) Explain working of VCO with the help of suitable block diagram and output waveforms. Draw the block diagram of any one application of PLL. (4)

C) Design a 6 - bit weighted - resistor DAC whose full-scale output voltage is -8V. The expected logic levels are 1 = 8V and 0 = 0V. Draw the circuit diagram of the same. What is the output voltage when the input is 110010? (3)

5) Explain working of dual-slope type ADC using suitable block diagram. (3)

A)

B) Explain working of successive approximation type ADC using an example. (4)

C) The data sheet of the REF101KM 10V precision voltage reference gives a typical line regulation of 0.001% / V, a typical load regulation of 0.001% / mA and a maximum thermal coefficient of 1ppm / °C. Find the variation of V_o brought by a) change of V_i from 13.5V to 28V; b) ±8mA change in I_o; c) temperature change from 0°C to 56°C. (3)

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