Question Paper

Exam Date & Time: 23-Jun-2022 (02:00 PM - 05:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
Second Semester Master of Engineering - ME(VLSI Design) Degree Examination - June 2022

Low Power VLSI Design [VLS 5202]

Marks: 100 **Duration: 180 mins.**

Thursday, June 23, 2022

Answer all the questions.

1)	Derive an expression for the switching power dissipation component in a CMOS circuit. Discuss how switching power can be minimized. (TLO 2.1) (10 Marks)	(10)
2)	What are the factors affecting leakage power in a CMOS circuit? Explain them with required graphs. (TLO 2.2) (10 Marks)	(10)
3)	Explain with diagrams, the following multiple V_{TH} techniques to suppress the sub-threshold leakage current: a) Multi-threshold CMOS (MTCMOS) b) Dual Threshold CMOS (TLO 3.2) (5+5 Marks)	(10)
4)	A CMOS processor has a rated supply voltage 1.5V and clock frequency 2GHz. Its average power consumption is 100W, which consists of 75W dynamic power and 25W static power. Assuming that the delay of a gate in the technology is proportional to VDD/(VDD - Vth), where the threshold voltage Vth = 0.5V. A low energy mode uses a lower supply voltage and a reduced frequency clock a) Determine the voltage and clock frequency that will minimize the average energy consumption per cycle. b) Compare the power consumption and energy per cycle for the rated and low energy modes. (TLO 3.2) (5+5 Marks)	(10)
5)	Explain with relevant diagrams, voltage scaling using Threshold Reduction approach for dynamic power reduction. (TLO 4.2) (10 Marks)	(10)
6)	What are the various ways of glitch reduction? Explain with relevant diagrams. (TLO 5.1) (10 Marks)	(10)
7)	What is Clock Gating? Explain latch-free and latch-based implementation of clock gating. (TLO 6.1) (10 Marks)	(10)
8)	Explain the operation of a Split Level Charge Recovery Logic(SCRL) NAND gate. (TLO 7.1) (10 Marks)	(10)
9)	Discuss the most popularly used logic optimization techniques for power reduction. (TLO 8.1) (10 Marks)	(10)
10)	a) Illustrate the operation of a low to high voltage domain level shifter. b) Write a short note on level shifter placement. (TLO 9.1) (5+5)	(10)

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