Question Paper

Exam Date & Time: 11-Aug-2022 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
Second Semester Master of Engineering - ME (VLSI Design) - Degree Examination (Make up) - August 2022

Universal Verification Methodology [VLS 5204]

Marks: 100 **Duration: 180 mins.**

Thursday, August 11, 2022

Answer all the questions.

1)	Define inheritance in Object Oriented Programming. Write a program for differentiating instantiation and inheritance. Explain the keywords this, super, and local with suitable examples.(TLO 2.2) (10 Marks)	(10)
2)	Describe package in Object Oriented Programming. Provide an example to elucidate its importance.(TLO 3.1) (10 Marks)	(10)
3)	Explain UVM field macros. Provide any five flags and their description. Give an example code for UVM object print using field macros.(TLO 3.2) (10 Marks)	(10)
4)	Explain UVM Message facilities with respect to severity, verbosity, and simulation handling behavior by giving suitable examples.(TLO 3.3) (10 Marks)	(10)
5)	Explain uvm_sequence_item class in UVM. Provide a program to describe create and sequence_item compare.(TLO 4.5) (10 Marks)	(10)
6)	Describe monitor in UVM component with the help of an example(TLO 4.3) (10 Marks)	(10)
7)	Mention the components of Universal Verification Component. Explain Registration and Construction using UVM factory. (TLO 5.1) (10 Marks)	(10)
8)	Explain configuration mechanisms. Compare create () and new () methods in UVM.(TLO 6.1) (10 Marks)	(10)
9)	Define UVM register abstraction layer. Give an example for	(10)

register and explain read & write and peek & poke methods(TLO 10.1) (10 Marks)

10) Explain TLM blocking put_port with the help of a UVM program (TLO 12.1) (10 Marks) (10)

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