Question Paper

Exam Date & Time: 01-Jul-2022 (02:00 PM - 05:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
Second Semester Master Engineering - ME (VLSI Design) Degree Examination - June 2022

Universal Verification Methodology [VLS 5204]

Marks: 100 **Duration: 180 mins.**

Friday, July 1, 2022

Answer all the questions.

1)	Illustrate a UVM program to display "Hello World!" with design under test, interface, environment, test, and top files.(TLO 1.2) (10 Marks)	(10)
2)	Define Parameterization and encapsulation in Object Oriented Programming. Write two separate programs to explain their significance. (TLO 2.3) (10 Marks)	(10)
3)	Explain uvm_object class and uvm_component class with examples(TLO 3.1) (10 Marks)	(10)
4)	Explain UVM Message facilities with respect to severity, verbosity, and simulation handling behavior by giving suitable examples.(TLO 3.3) (10 Marks)	(10)
5)	Explain the functionality of uvm_driver with example (TLO 4.5) (10 Marks)	(10)
6)	Explain UVM factory overrides with examples.(TLO 6.1) (10 Marks)	(10)
7)	Explain uvm_sequence_item class in UVM. Provide a program to describe create and sequence_item pack. (TLO 8.3) (10 Marks)	(10)
8)	Define UVM register layer. Give an example for register and explain read & write and peek & poke methods (TLO 10.2) (10 Marks)	(10)
9)	Explain First In First Out concept in UVM TLM with a program (TLO 12.1) (10 Marks)	(10)
10)		(10)

Explain TLM blocking get_port with the help of a UVM program (TLO 12.2) (10 Marks)

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