Exam Date & Time: 25-Jul-2022 (02:00 PM - 05:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

FOURTH SEMESTER B.TECH MAKEUP EXAMINATIONS, JULY 2022

DIGITAL SYSTEM DESIGN [BME 2253]

Marks: 50 **Duration: 180 mins.**

A

Answer all the questions.

Instructions to Candidates: Answer ALL questions Missing data may be suitably assumed

1) Differentiate the full-custom and semicustom Application Specific Integrated Circuit (ASIC). Write an advantage and disadvantage of each of above ASIC. (3)

A)

B) Design a two input CMOS OR gate with a neat circuit, mention the details of pullup and pull-down transistors. Verify the operation of gate considering possible input combinations. (3)

C) Design multiplexer using TG and other basic gates. Explain its operation. (4)

2) State Shannon's expansion theorem considering three logic variables. Design a MUX based circuit by applying the theorem to find the co factors of the following function with respect to variable w2: (4)

A)

f (w1,w2,w3) = w1w2+w1w3+w2w3.

B) Design an AND-OR plane of a PLA considering NMOS programmable switches to realize the following function: Y= ABC +B'C. Draw the diagram and explain the operation of the given planes. (3)

C) Explain the architecture of PAL. Differentiate PAL and Complex PLD. (3)

3) Design a CMOS inverter circuit and explain how it is different from a NMOS inverter. (3)

A)

B) Design a Verilog HDL module for realizing the following function using gate primitive: F= AB+AB'+C. Show that instance of the specified module are created in two styles. Note: Write comments on each line. (3)

C) Discuss the architecture of a CPLD along with its advantage and disadvantage. (4)

4) Describe the FPGA configurable logic block (CLB) with a neat diagram. How it is different from CPLD. (4)

A)

B) Design 2 input LUTs design, for realising the given function, F= AB+ CD'. Write the details of function table and the LUT used for each stage. (3)

C) Illustrate the role of Verilog HDL in the digital system design. Explain how these HDL is different from a programming language like C++ or python. (3)

5) Design a Verilog HDL module to synthesis a full adder circuit using assignment statements. (3)

A)

B) Explain how always block statement are used in the design of a basic sequential circuit in Verilog HD. (3)

C) Discuss the two types of module instantiation. How they are different. Consider an example and create a of a module instance. (4)

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