Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

DEPARTMENT OF MECHATRONICS

IV SEMESTER B.TECH. (MECHATRONICS)

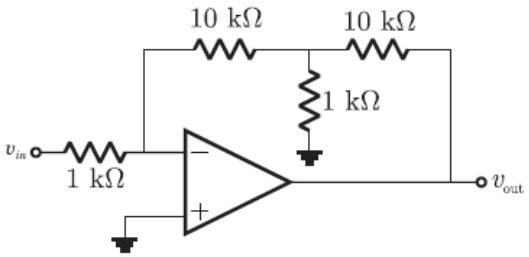
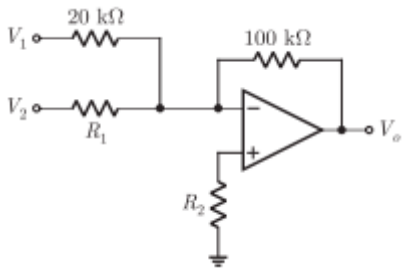
END SEMESTER EXAMINATIONS, JUNE 2022

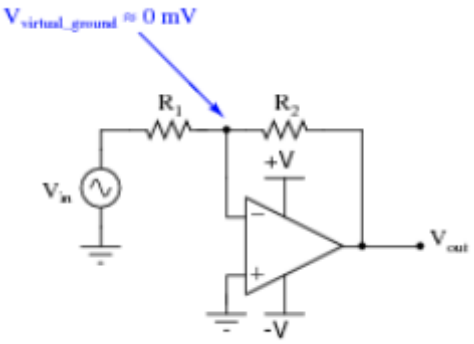
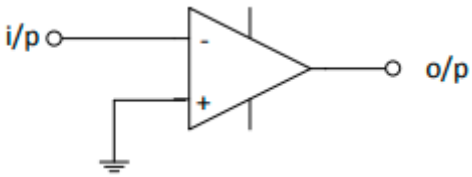
SUBJECT: LINEAR INTEGRATED CIRCUITS & APPLICATIONS [MTE 2254]

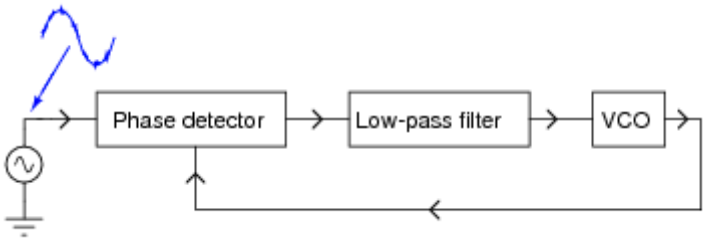
Time: 3 Hours **MAX. MARKS: 50**

Instructions to Candidates:

- Answer **all questions**.

Q. No		M	CO	PO	LO	BL
1A.	Assuming the operational amplifier to be ideal, Obtain the gain $\frac{V_{out}}{V_{in}}$ for the circuit shown in figure 1A.  Figure 1A	**3**	**1**	**1**	**1**	**3**
1B.	Consider the opamp circuit shown in figure 1B.  Figure 1B a) If V_1 =0.2V, V_2 =0.6V and V_0 = -7V and the opamp is ideal. Calculate the value of R1. b) Let V_1 =V_2 =$V_c sin2\pi ft$ and R_1 = 20kΩ. The opamp has a slew rate of 0.5V/µS with its parameter being ideal. Obtain the value of Vc and Frequency F.	**4**	**1**	**1**	**1**	**3**

	c) Let V1=V2 and R1 = 20kΩ. Assume that opamp is ideal except for non-zero input bias current. Obtain the value R_2 for which output voltage of opamp to be zero.					
1C.	The junction between the two resistors and the inverting input of the operational amplifier is often referred to as a virtual ground, the voltage between it and ground being (almost) zero over a wide range of circuit conditions: a) If the operational amplifier is driven into saturation, though, the "virtual ground" will no longer be at ground potential. Explain the reason for this , and mention the condition(s) which may cause this to happen.  Figure 1C	**3**	**1**	**2**	**2**	**4**
2A.	If the input to the circuit of figure 2A is a sine wave. Determine the output . Justify the reason for the obtained output.  Figure 2A	**2**	**1**	**1**	**1**	**4**
2B.	The input of a certain regulator increases by 3.5 V. As a result, the output voltage increases by 0.042 V. The nominal output is 20 V. Determine the line regulation in both % and in %V.	**2**	**3**	**1**	**1**	**3**
2C.	Justify the correctness or otherwise of the following statements: 1. Switching regulators are more efficient than linear regulator making them ideal for low voltage high current applications. 2. The voltage drop of switching regulator is similar to a resistor voltage drop. 3. Sample-and-hold circuits in analog-to digital converters (ADCs) are designed to stabilize the input analog signal during the conversion process.	**6**	**3**	**2**	**2**	**4**
3A.	Explain the working of two basic linear regulators.	**3**	**3**	**1**	**1**	**2**

3B.	The PLL acts like a low-pass filter, the high-frequency VCO noise mostly get rejected. Justify the correctness of the statement with the working principle.	**4**	**3**	**2**	**2**	**4**
3C.	Suppose that a "noisy" AC signal of constant frequency is connected to the input of a phase-locked loop circuit:  Characterize the output waveform generated by the VCO. Will it be "noisy" as well? Justify.	**3**	**3**	**3**	**5**	**4**
4A.	In a R-2R ladder type DAC if a switch status is '0', 0V is applied and if a switch status is '1', 5V is applied to the corresponding terminal of the DAC.Obtain the output voltage (V_0) for the switch status S_0 = 0, S_1= 1, S_2 = 1.	**2**	**4**	**1**	**1**	**3**
4B.	Mention the major advantage of the R/2R ladder digital-to-analog, as compared to a binary-weighted digital-to-analog converter?	**3**	**4**	**1**	**1**	**2**
4C.	A 4-bit successive approximation type ADC has a full scale value of 15V. Obtain the sequence of the states, if SAR traverse, for the conversion of an input of 8.15V.With the help of a block diagram explain the working of SAR.	**5**	**4**	**1**	**1**	**3**
5A.	Design a flow chart for building time monitored touchless automatic sanitizer dispenser using 555 timer.	**3**	**2**	**3**	**5**	**5**
5B.	Highlight the need of an hour to develop an eco friendly process for the recycling of waste printed circuit board.	**3**	**1**	**7**	**5**	**4**
5C.	Discuss any four performance parameter for assessing the working of a industry grade voltage regulators.	**4**	**3**	**1**	**1**	**2**