Question Paper

Exam Date & Time: 29-Jun-2022 (02:00 PM - 05:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
Second Semester Master of Engineering - ME (Embedded Systems) Degree Examination - June 2022

Multicore Program Optimization Elective -2 [ESD 5235]

Marks: 100 **Duration: 180 mins.**

Wednesday, June 29, 2022

Answer all the questions.

1)	Consider the following 3 DLX instructions: (i) STORE (ii) BRANCH (iii) ADD. Consider the 5 stages of the DLX machine architecture, Indicate what actions take place in each stage for the above mentioned instructions. [TLO1.1]	(10)
2)	Explain the various ways by which we can reduce branch hazards? [TLO1.2]	(10)
3)	Explain direct mapping, set associative and the fully associative address mapping techniques. Provide one common example to illustrate all the 3 techniques. [TLO1.3]	(10)
4)	Design the average memory access time for the following caches [TLO1.3 (i) 32 KB unified cache (ii) 16 KB Instruction and 16 KB data cache.Assume a hit takes one Clock cycle. Miss penalty takes 50 clock cycles. Load and store take one extra clock cycle in case of unified cache. About 75% of memory accesses are instruction eferences. Given that Miss rate for 16KB instruction cache is 0.64%, Miss rate for 16KB data cache is 6.47% and Miss rate for 32kb Unified cache is 1.99%, compare the miss rates and the average memory access times in the above two cases.	(10)
5)	Explain in detail what do you understand by hardware prefetching of data? How it is different from compiler controlled prefetching? [TLO1.3]	(10)
6)	Explain, compare and contrast the following 4 terms: SISD, SIMD, MISD, MIMD. [TLO1.2]	(10)
7)	Assume a multiprocessor system consists of 3 processors, p1, p2, and p3, each having its own local cache, c1, c2, and c3, respectively. The coherence among the caches is maintained using MSI protocol. Describe the state transitions of all the three caches for the following memory operations on a memory block u. [TLO2.1] (i) P1 reads U (ii) P1 writes to u (iii) P2 Reads to u (iv) P2 writes to u (v) P3 Writes to u (vi) P3 reads u (vii) P1 wites to u	(10)
8)	Explain the following clauses with examples (5*2m)=(10)m [TLO3.2] i. atomic ii. master iii. ordered iv. nowait v. critical	(10)
9)	Discuss the different multiprocessing techniques [TLO3.2]	(10)

10) Describe comprehensively key features of various performance tools. [TLO3.1] (10)

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