Question Paper

Exam Date & Time: 29-Jun-2022 (02:00 PM - 05:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
Second Semester Master of Engineering - ME (VLSI Design) Degree Examination - June 2022

Physical Design Elective -2 [VLS 5234]

Marks: 100 **Duration: 180 mins.**

Wednesday, June 29, 2022

Answer all the questions.

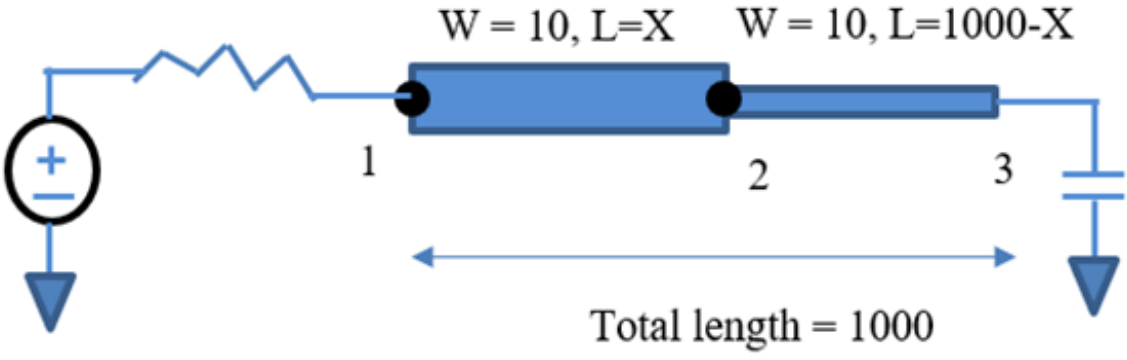
1) List and explain the properties of static CMOS and dynamic CMOS logic gates (TLO 1.1) (10 Marks) (10)

2) Explain the contents of a technology file? Indicate ASIC width & height and Core width and height with the help of a diagram (TLO 2.4) (10 Marks) (10)

3) List the goals, Objectives, Inputs and Outputs of a placement tool? Describe Global placement in detail (TLO 3.1) (10 Marks) (10)

4) Explain Detail Routing in physical design stage. (TLO 5.4) (10 Marks) (10)

5) Compute the value of X so that the delay value at the load is 530. The total length of the wire from point 1 to 3 is 1000. The driver resistance is 500.Load Capacitance is $1x10^{-4}$, (10)
R = 500 * L/W,
C = ($2x10^{-6}$) L * W.
(TLO 6.1) (10 Marks)



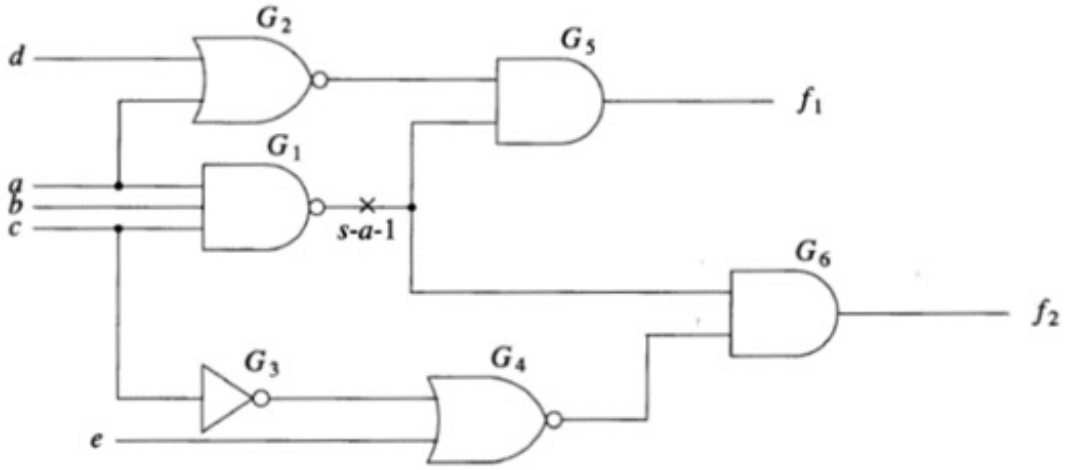
6) Explain the different types of capacitance considered in the (10)

extraction procedure after the layout? (TLO 7.2) (10 Marks)

7) Describe the significance of Testing in VLSI. Differentiate Verification and Testing (TLO 8.1) (10 Marks) (10)

8) What are the advantages of modelling physical fault as a logical fault? Find out the collapse ratio for a two input XOR gate built using NOR gates only (TLO 8.4) (10 Marks) (10)

9) Explain the sensitize, propagate and backtracking with respect to the fault shown in the circuit (TLO 8.4) (10 Marks) (10)



10) Explain pseudo-random pattern generation method of testing in VLSI (TLO 8.8) 10 Marks) (10)

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