Question Paper

Exam Date & Time: 06-Jan-2023 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

FIRST SEMESTER B.TECH. EXAMINATIONS - JANUARY 2023
SUBJECT: ECE 1071 / ECE-1071 - BASIC ELECTRONICS

Marks: 50 **Duration: 180 mins.**

Answer all the questions.

1A)	Obtain an expression for the drain current of MOSFET in terms of 'V_{GS}', 'V_{DS}', and the dimension of the device. Also, plot the VI characteristics of the device indicating all the salient features on it.	(4)
1B)	Plot the VI characteristics of a Zener diode. Explain the different types of regulations that can be found in a Zener regulator with a neat circuit diagram and relevant equations.	(3)
1C)	Calculate the static and dynamic resistance of a PN junction Germanium diode at a temperature of 50^0 C, when the applied voltage is 0.25V and reverse saturation current is 10 µA.	(3)
2A)	A sinusoidal voltage of 130V peak-to-peak from the secondary of the transformer is applied to a half-wave rectifier, with a load resistance of 1kΩ. If the cut-in voltage of the diode is 0.7V and the forward resistance of the diode is 30Ω, find the values of the following. i) DC and RMS values of the load current. ii) DC output power and AC input power.	(4)
2B)	Draw the Zener voltage regulator circuit. Given, the series resistance connected in the circuit is 2kΩ and the load applied is 4kΩ. Input voltage is varied between (31±9) V. Zener breakdown voltage is 10V. Find the minimum and maximum value of current through the Zener.	(3)
2C)	With a neat circuit diagram, explain the working of a full wave bridge rectifier with a capacitor filter. Draw the corresponding input and output waveforms.	(3)
3A)	A (7,4) bit Hamming code received is 0100111($P_1P_2D_3P_4D_5D_6D_7$), considering even parity. Check for errors in the received code and if there is an error, write the corrected code, Also represent the corrected code in 8421 BCD code.	(4)
3B)	The inputs V_1=60µV and V_2=30µV is given to the non-inverting and inverting terminals of an OPAMP, respectively. The common mode gain is 40dB and CMRR is 60dB. Calculate the output voltage. Also, Determine the output voltage when V_1=V_2=30µV is given as input.	(3)
3C)	Realize an op-amp inverting integrator with RC=1 second, and input is a step voltage of 2V. Determine the output voltage at t=4 second and sketch the output waveform.	(3)
4A)	Simplify the following SOP expression using K-Map and implement using NAND gates only f (A, B, C, D) = ∑m (0,1,4,5,6,7,9,11,15)+ ∑d (10,14).	(4)
4B)	Realise a 3-bit up counter using the positive edge triggered JK flip flops. Draw the timing diagram for the same.	(3)
4C)	With a neat logic diagram and truth table, explain the working of SR flip-flop, implemented using only NAND gates. Mention the limitation of SR flip-flop.	(3)
5A)	Certain AM transmitter radiates 12kW of power with carrier unmodulated and 15.250kW of power when carrier is sinusoidally modulated. Calculate the modulation index. If another sine wave corresponding to 60% modulation is transmitted simultaneously, determine the total power radiated.	(4)
5B)	Write the equation for Frequency Modulated signal in time domain for a sinusoidal modulating signal. Determine the bandwidth and modulation index of FM signal required to transmit 12 kHz, 3V	(3)

peak amplitude signal with frequency sensitivity 18 kHz/V using Carson's rule.

5C) Define sampling theorem. Consider an analog signal, (3)
$x(t)=15\cos(15\pi t)+10\sin(100\pi t)+5\cos(300\pi t)$.
Determine the minimum sampling rate required to reconstruct the signal.

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