Question Paper

Exam Date & Time: 10-Dec-2022 (02:30 PM - 05:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

FIRST SEMESTER B.TECH END SEMESTER EXAMINATIONS, NOV 2018

DIGITAL ELECTRONICS [BME 2153]

Marks: 50 **Duration: 180 mins.**

A

Answer all the questions. Section Duration: 180 mins

Instructions to Candidates: Answer ALL questions Missing data may be suitably assumed

1) Write the a) Min Terms b) Max Terms c) Standard SOP Form d) Minimal SOP e) Canonical POS Form f) Minimal POS; (5)

A)

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

for the given Truth Table.

B) Discuss 4-bit Johnson's counter with the help of D flip flop and truth table. (3)

C) Determine the grey code equivalent of the given binary number a) 1001 b) 1010. (2)

2) Illustrate the following using Active high and Active low decoder $F(A,B,C) = \sum m(0,2,3,7)$ and $G(A,B,C) = \sum m(1,4,6,7)$ (4)

A)

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B) Design a Full subtractor using 1:8 De-MUX (4)

C) Describe 1 bit comparator with help of logic diagram and Truth table. (2)

3) Explain S-R latch using NOR gate with relevant logic diagram and Truth table. (4)

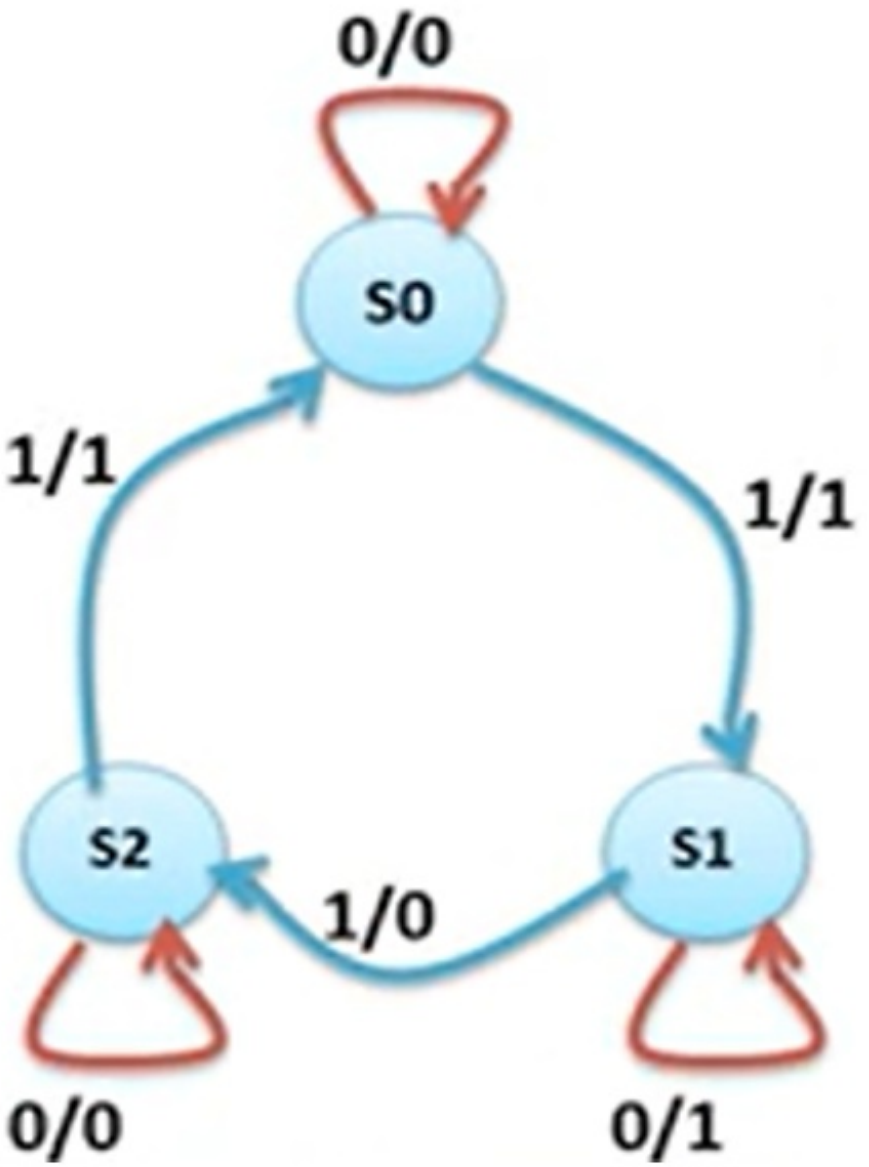
A)

B) Illustrate Master Slave J-K Flip flop using NAND gates. (4)

C) Explain T flip flop with relevant logic diagram and Truth table. (2)

4) Determine the ASM chart (5)

A)



for the given state diagram.

B) Explain Moore machine with help of block diagram and T Flip flop. (3)

C) Summarize any two differences between Moore and Mealy machine. (2)

5) Design CMOS NAND gate with the relevant logic diagram and truth table. (4)

A)

B) Design TTL NAND gate with the relevant logic diagram and truth table. (4)

C) Explain any two characteristics of digital logic family. (2)

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