Question Paper

Exam Date & Time: 25-Jan-2023 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

THIRD SEMESTER B.TECH END SEMESTER MAKE- UP EXAMINATIONS, JAN 2023

DIGITAL ELECTRONICS [BME 2153]

Marks: 50 **Duration: 180 mins.**

A

Answer all the questions.

Instructions to Candidates: Answer ALL questions Missing data may be suitably assumed

1) Write the a) Standard POS and b) Minimized POS (2)

A)

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	0

for the given Truth Table.

B) Discuss 4-bit Ring counter with the help of D flip flop and truth table. (4)

C) Deduce half adder using NOR gate only. (4)

2) Implement the following using Active high and Active low decoder $F(A,B,C) = \sum m(0,2,3,7)$ and $G(A,B,C) = \sum m(1,4,6,7)$ (4)

A)

B) Implement a 1 bit full adder using 4:1 MUX. (4)

C) Describe 1 bit comparator with help of logic diagram and Truth table. (2)

3) Explain S-R latch using NAND gate with relevant logic diagram and Truth table. (4)

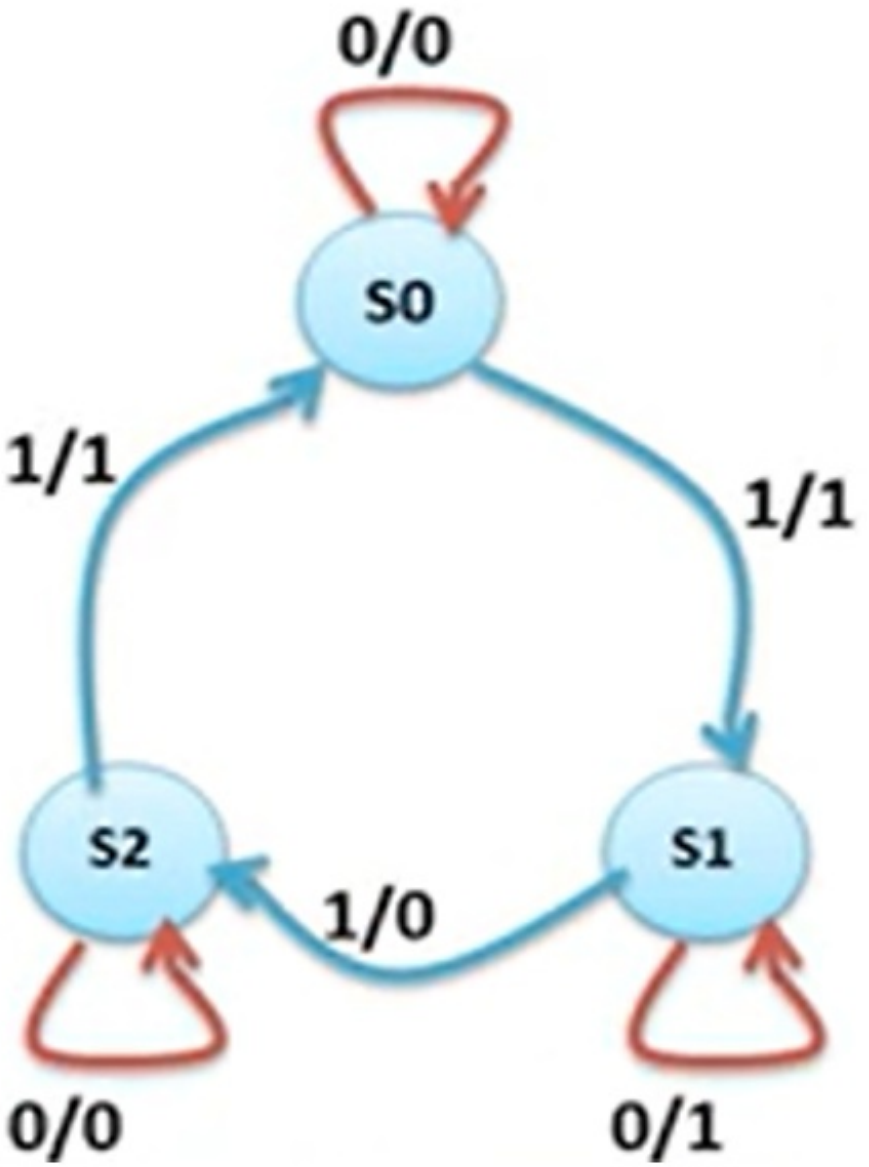
A)

B) Illustrate J-K Flip flop using NAND gates with relevant logic diagram and Truth table. (4)

C) Explain D flip flop with relevant logic diagram and Truth table. (2)

4) Determine the Moore model (5)

A)



for the given state diagram.

B) Explain Mealy machine with the help of block diagram and T Flip flop. (3)

C) Mention any two differences between Moore and Mealy machine. (2)

5) Explain any four characteristics of digital logic family. (4)

A)

B) Determine TTL NAND gate with the relevant logic diagram and truth table. (4)

C) Write a short note on digital logic family. (2)

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