Question Paper

Exam Date & Time: 19-Dec-2022 (02:30 PM - 05:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

THIRD SEMESTER B.TECH. (ELECTRONICS AND COMMUNICATION ENGINEERING) EXAMINATIONS - DECEMBER 2022
SUBJECT : ECE 2151 - ANALOG ELECTRONIC CIRCUITS

Marks: 50 **Duration: 180 mins.**

Answer all the questions.

1A) We wish to design the source follower shown in FIG.Q1(A) for a voltage gain of 0.8. If W/L = (30/0.18) and λ = 0, determine the required gate bias voltage. Assume $\mu_n C_{ox}$ = 200μA/V^2, V_{TH} = 0.4V. (4)

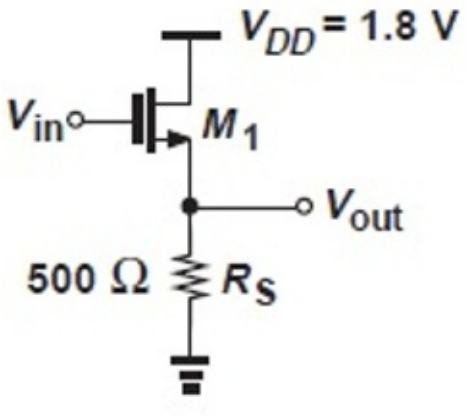


FIG.Q1(A)

1B) A MOSFET is biased at a drain current of 0.5 mA. If $\mu_n C_{ox}$ = 100 μA/V^2, W/L = 20, and λ = 0.1V^{-1}, calculate its small-signal parameters g_m & r_o and voltage gain. (3)

1C) The common-gate stage shown in FIG.Q1(C) must provide a voltage gain of 4 and an input impedance of 50Ω. If I_D = 0.5 mA, and λ = 0, determine the values of R_D and W/L. (3)

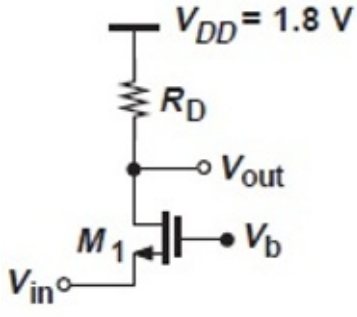


FIG.Q1(C)

2A) A MOS differential amplifier is operated at a total current of 0.8 mA, using transistors with a W/L ratio of 100, $\mu_n C_{ox}$ = 0.2 mA/V^2 , λ = 0.05V^{-1} and R_D = 5KΩ. Find the over drive voltage, transconductance 'g_m', output resistance 'r_o' and differential voltage gain 'A_d'. (4)

2B) Design a NMOS cascode with (W/L) = 32 and a current of 0.5 mA. Assume M1 and M2 to be identical, $\mu_n C_{ox}$=100μA/V^2 and λ = 0.1V^{-1}. Also, find the output resistance. (3)

2C) Calculate 'I_{copy}' in the circuit shown in FIG.Q2(C). Assume all the MOSFETs in saturation and λ = 0. (3)

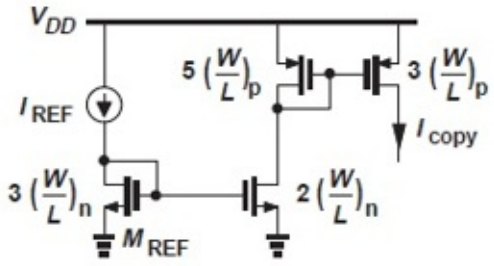


FIG.Q2(C)

3A) Find the differential gain, common mode gain and CMRR of the circuit shown in FIG.Q3(A). Assume λ≠0 and ideal current source 'I_{SS}'. (4)

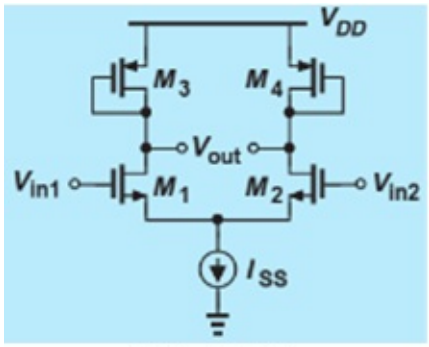


FIG.Q3(A)

3B) Estimate the input and output poles of the circuit shown in FIG.Q3(B). Assume λ=0 and neglect internal capacitance of MOSFET. (3)

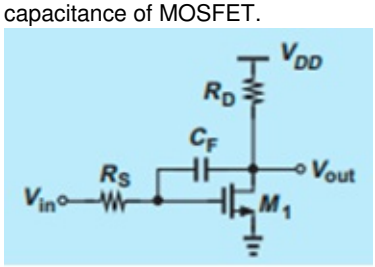
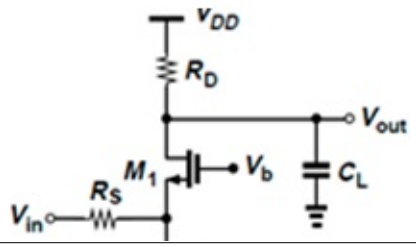


FIG.Q3(B)

3C) For the amplifier shown in FIG.Q3(C), $g_m = (150\Omega)^{-1}$, $\lambda = 0$, $R_D = 2k\Omega$, $R_S = 200\Omega$, Cin = 1μF, and $C_L = 43nF$. Neglecting the MOSFET capacitance, sketch the frequency response of the amplifier indicating the pole frequencies. (3)



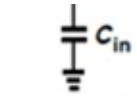


FIG.Q3(C)

4A) Determine the closed loop gain, I/O impedances of the circuit shown in FIG. Q4(A). (4)

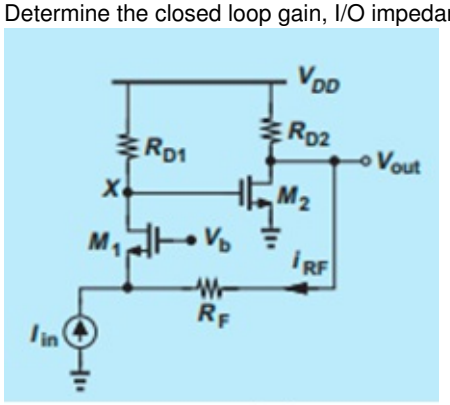


FIG.Q4(A)

4B) Determine the polarity of feedback for the circuit shown in FIG.Q4(B) with justification. (3)

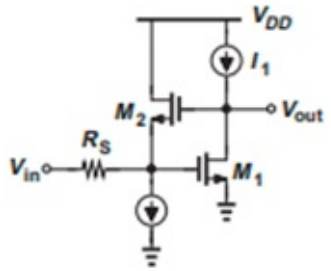


FIG.Q4(B)

4C) For the block diagram shown in FIG. Q4(C), Identify the feedback topology and obtain the expressions for I/O impedances. (3)

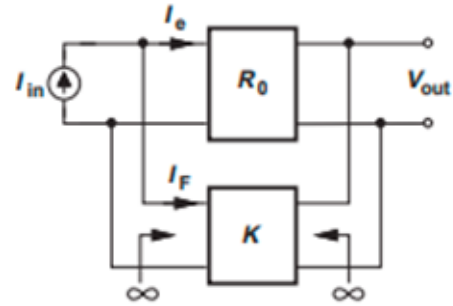


FIG.Q4(C)

5A) For the circuit shown in FIG.Q5(A), obtain the expressions for minimum gain required for oscillation and the frequency of oscillation. (4)

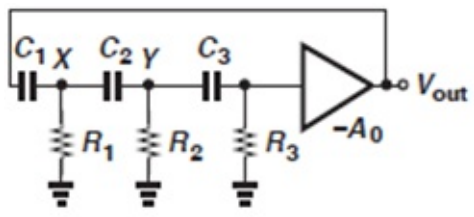


FIG. Q5(A)

5B) Explain the working principle of Hartley Oscillator with a neat circuit diagram. Also, obtain its frequency of oscillation for $L_1 = L_2 = 1mH$ and $C = 1\mu F$. (3)

5C) Obtain an expression for efficiency of Class - B push pull power amplifier. (3)

[illegible] Obtain an expression for efficiency of Class – B push pull power amplifier [illegible]

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