Question Paper

Exam Date & Time: 08-Dec-2022 (02:30 PM - 05:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

THIRD SEMESTER B.TECH. (ELECTRONICS AND COMMUNICATION ENGINEERING) EXAMINATIONS - DECEMBER 2022

SUBJECT : ECE 2152 - COMPUTER ORGANIZATION AND ARCHITECTURE

Marks: 50 **Duration: 180 mins.**

Answer all the questions.

1A)	For the expression X = (A-B/C)/(D+E*F - G/H), write the program for register based, accumulator based and stack based machine. Assume source and destination operands are memory locations.	(5)
1B)	With the 12 bit instruction length and 4 bit address field, verify the possibility to have fourteen 2-address, thirty 1-address and twenty four 0-address instructions.	(3)
1C)	With the help of a block diagram explain the working of stack-based processor.	(2)
2A)	Explain the working of carry look ahead adder (CLA) circuit. Using 4 bit CLA as building block design a 16-bit CLA. Also, calculate worst case add time of 16-bit CLA.	(5)
2B)	Design a fast 8 x 8 multiplier using 4 X 4 non additive multipliers and Wallace tree adders.	(3)
2C)	List the disadvantages of array multipliers. How is it overcome by Booth's and Modified Booth's algorithms? Explain.	(2)
3A)	Design a microprogrammed control unit for Booth's multiplier by giving the RTL code. Explain the control memory organization of Booth's multiplier with a neat diagram.	(5)
3B)	Build the hardware to implement each of the following register transfers: i) If Q[1]=0 AND Q[0]=1 then A←A+1 else A←A-1 ii) If Q[1:0]=01 OR Q[1:0]=10 then A←B Assume A, B and Q are 4-bit registers.	(3)
3C)	Convert the following decimal numbers to 32-bit IEEE floating point representation. Write the result in hexadecimal format. a) 45.125 b) 0.0125	(2)
4A)	Distinguish the difference between maskable and non-maskable interrupts. Explain with neat diagrams, software polled approach for connecting multiple interrupts to a single interrupt line. List its advantages and disadvantages.	(5)
4B)	A computer system needs a 1K X 8 RAM. Assuming 256 X 4 RAM chips are available, show how to build required RAM. Draw a neat logic diagram of your implementation.	(3)
4C)	A certain memory system has a 32MB main memory and a 64 KB Cache. Block are 16 bytes in sizes. Show the main memory address format to determine the length of TAG, Cache line number and WORD fields for the Direct mapping technique.	(2)
5A)	What is Superscalar architecture? Explain in detail the characteristic features of superscalar architecture.	(5)
5B)	What is CISC architecture? Explain its characteristic features.	(3)
5C)	A four-stage pipeline has stage delays as 40, 60, 90, and 70 ns respectively. Given latch delay is 5 ns.	(2)

Calculate,

i) Pipeline cycle time
ii) Non-pipeline execution time

-----End-----