Question Paper

Exam Date & Time: 10-Dec-2022 (02:30 PM - 05:30 PM)



MANIPAL ACADEMY OF HIGHER EDUCATION

THIRD SEMESTER B.TECH. (ELECTRONICS AND COMMUNICATION ENGINEERING) EXAMINATIONS - DECEMBER 2022 SUBJECT : ECE 2153 - DIGITAL SYSTEM DESIGN

Marks: 50

Duration: 180 mins.

Answer all the questions.

1A)

Figure Q1A shows operation of 2-bit adder. A0, A1, B0, B1 and S0,S1,S2 are inputs and outputs (4) respectively. Carry0 is an intermediate signal. Implement Half-adder and Full-adder block using appropriate decoders with active-High outputs and basic gates.



Figure Q1A

1B)	Design a code converter circuit to convert 3-bit Gray code to Binary code.				
1C)	Construct the TTL circuit for: (i) NOT gate (ii) NAND gate.				
2A)	What are the universal gates? Simplify the following Boolean expression using Karnaugh map and draw the logic circuit using only NAND gates $F(A,B,C,D)=\Sigma m(6,7,8,9,10,12)+d(2,5,13)$				
2B)	Derive the characteristic equation of P-Q flipflop. The characteristics table of P-Q flipflop is as follows. Convert P-Q flipflop to D flipflop				(3)
	Р	Q	Output (Q)		
	0	0	Invalid		
	0	1	Toggle		
	1	0	Set (1)		
	1	1	Reset (0)		

2C)

Design a Mealy overlapping sequence detector that detects sequence 101 using D flipflop and

necessary gate.

3A)	Implement 1111 overlapping sequence detector using Mealy model and draw the circuit diagram using D- flip flop and necessary logic gates.	(4)
3B)	Construct a 2-bit synchronous up counter using T-flip flop.	(3)
3C)	Write a dataflow Verilog code for 2-to-4 decoder with active low enable input and active low outputs.	(3)
4A)	Write the structural Verilog code for 8:1 multiplexer using 2:1 multiplexer.	(4)
4B)	Write the Verilog code for 3 input NAND gate using User defined primitive.	(3)
4C)	Write the sequential Verilog code for positive edge triggered J-K Flipflop.	(3)
5A)	Implement a 4-bit SISO register using Xilinx CLB.	(4)
5B)	Implement F = Σ m (1,3,5,6) using ACT-1 module.	(3)
5C)	Implement a BCD to XS-3 code conversion circuit using PROM.	(3)

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