Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

III SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, DECEMBER 2022

ANALOG SYSTEM DESIGN [ELE2151]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 16 December 2022** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.
- Steps must be clearly shown

Q1A A MOS is being fabricated with, t_{ox}=8 nm, μ_n= 450 cm^2/V ε_{ox}=34.53*10^{-12}, (W/L) = 8 μm/0.8 μm and V_{th} = 0.7 V

i. Find Oxide capacitance(C_{ox}), process transconducance parameter (k_n')
ii. Calculate the values of overdrive voltage (V_{ov},) and V_{GS} needed to operate the transistor in the saturation region with a DC bias current of 100 μA.
iii. Determine the gate to source voltage (V_{GS}) required to operate the MOSFET as 1 kΩ voltage dependent resistor.

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Q1B An IC chip with several amplifier stages, a constant DC current (reference current) is to be generated at one location and is to be replicated at other location. This DC replicated current will be used for biasing amplifiers. Using the methodology of current steering (mirror), how can you achieve this? Justify your reasoning with circuit diagram and equations. **3**

Q1C Determine the bandwidth of 3 cascaded identical amplifier with each of them having 1 KHz as lower cut off frequency and 15 KHz as higher cutoff frequency. **2**

Q2A Determine the bandwidth of RC coupled amplifier shown in the below Fig. Q2A. Also draw the small signal model of the same. **4**

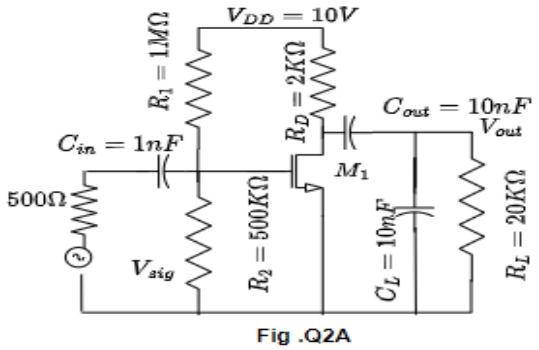

Fig .Q2A

2B Develop the small signal model hence determine the voltage gain of source follower (voltage Buffer) circuit. The source follower parameters are V_{th} =1 V, I_{DQ}=10 mA, V_G=7.46 V and R_S=500 Ω. **3**

2C Design a 555 timer negative edge triggered monostable multivibrator to produce a pulse 1 ms, hence draw the relavent circuit schematic. Draw the voltage waveforms at pin 6 and 3 when the monostable circuit is triggered by a 500 Hz square wave. Assume C=0.1 μF **3**

Q3A Derive an expression for the output voltage V_{out} of the amplifier circuit shown in Fig. Q3A. Hence find the value of V_R required to get, $0 \leq V_{out} \leq 3.3$ V for $-5V \leq (V_2-V_1) \leq +5$ V.

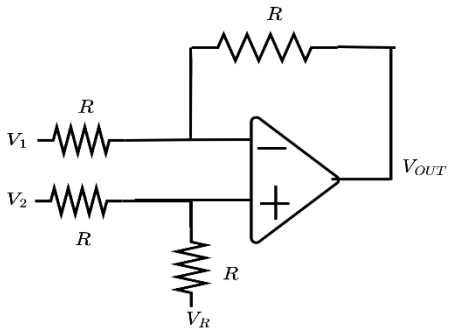

Fig : Q3A **4**

3B Using Op-amps, design a 1 kHz, 6 V (peak to peak) triangular wave generator. Assume C=0.01μF **3**

3C With a neat circuit schematic design a second order Butterworth low pass filter to filter the harmonics with frequency greater than 10 KHz. Assume C=0.01 μF and ±VDD=±12 V. **3**

Q4A For the cascaded amplifier shown in Fig.Q4A, I_{D1}=5 mA, V_{G1}=3.33 V, I_{D2}=10 mA, and threshold voltages of M1& M2 is V_{th}=0.2 V.

i. Draw the small signal equivalent circuit.

ii. Determine individual stage gains and overall gain.

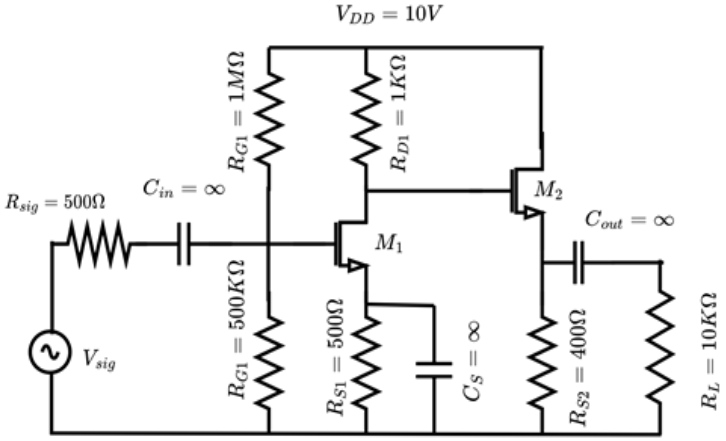

Fig.Q4A **5**

Q4B With neat diagram explain the working of an all-pass filter **2**

Q4C A MOS differential pair operated at a bias current of 5 mA employs transistors with (W/L) =10 and $\mu_n C_{ox}$=10 mA/V², using R_D=1 kΩ and R_{SS}= 50 kΩ.

i. Find the differential gain, the common mode gain if the output is taken as single-ended and the circuit is perfectly matched.

ii. If we supply differential input voltage v_{id}=500 mV assess OPAMP's mode of operation (linear mode or non- linear mode). **3**

Q5A From the fundamental determine the conversion efficiency of a class A power amplifier. **4**

Q5B A class B power amplifier providing 22 V peak signal to a 5 Ω load (speaker) and a power supply of $|V_{DD}|=|V_{SS}|$=24 V, determine the input power, output power, and circuit efficiency. **3**

Q5C Small signal equivalent circuit of an amplifier is as shown in the Fig.Q5C. Calculate the mid-band gain, input and output miller capacitances and evaluate its effect on amplifier band width.

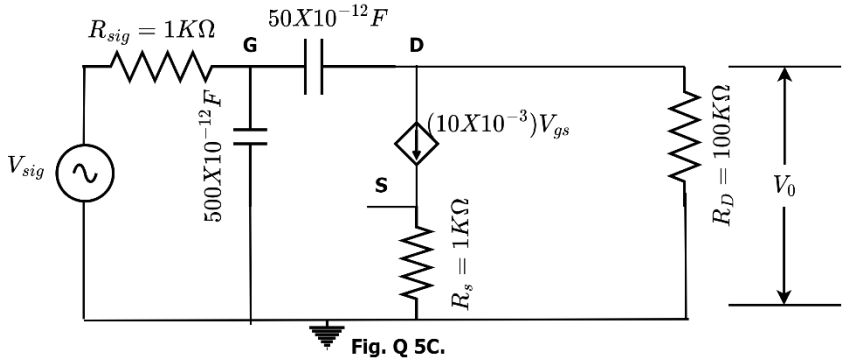

Fig. Q 5C.

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