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# MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
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## III SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

## END SEMESTER EXAMINATIONS, DECEMBER 2022

## DIGITAL SYSTEM DESIGN [ELE 2152]

REVISED CREDIT SYSTEM

**Time: 3 Hours** **Date: 10 December 2022** **Max. Marks: 50**

**Instructions to Candidates:**

- Answer **ALL** the questions.
- Missing data may be suitably assumed.
- Steps must be clearly shown

**1A** Obtain the simplified Boolean expression for the following Karnaugh Map. **2**

Table Q.1

| xy / z | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | A | A | C |
| 1 | B | 1 | ∅ | $\bar{B}$ |

**1B** A burglar alarm is designed so that it senses four input signal lines. Line A is from the secret control switch, line B is from a pressure sensor under a steel security safe in a locked closet, line C is from a battery powered clock, and line D is connected to a switch on the locked closet door. The following conditions produce a logic 1 signal on each line.

A: The control switch is closed.
B: The steel security safe is in its normal position in the closet.
C: The clock is between 10:00 and 16:00 hours (banking Hours)
D: The closet door is closed.
Analyze the given problem statement and write the switching expression for the burglar alarm that produces a logic 1 (rings a bell) when the security safe is moved and the control switch is closed, or when the closet is opened after banking hours, or when the closet is opened with the control switch open. Design the circuit using two numbers of 4:1 multiplexers and residual gates. **3**

**1C** Find a minimal sum of product expression for the following function using Quine Mc-Cluskey method.

$F(A, B, C, D) = \sum m(2, 3, 4, 5, 6, 8, 11, 12, 13) + d(10, 14)$ **5**

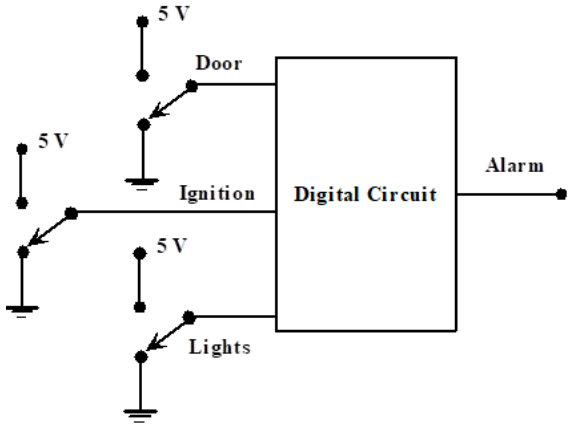
**2A** Show how $F = A + B + \bar{C}$ can be implemented using only 2 gates (one 2 input NAND gate and one 2 input NOR gate). **2**

**2B** Consider the automobile alarm circuit shown in the figure. The switches are used to represent the status of the door, ignition and headlights. Design a circuit to activate the alarm whenever any one or both of the following conditions exists:

- The headlights are ON while ignition is OFF.
- The door is open while the ignition is ON.

Implement the circuit using 3:8 active low decoder. Use minimum number of ICs in your implementation.

Figure Q.5




**3**

**2C** Design a 3-bit even number synchronous up counter using JK flipflops. **5**

**3A** AB Flip-flop has a characteristic equation $Q^+ = BQ + A\bar{Q}$,
Construct AB Flip-flop using T flip-flop, where A, B are the flip flop synchronous inputs, Q is the present state and Q+ is the next state. **2**

**3B** Design a 4-bit logic circuit using IC 74LS283 (4 – bit binary adder IC) to obtain 4-bit Binary sum output S, and F is the 4 bit input. When Switch S=1 circuit should perform S = F+'9', else should perform 1's compliments of F. **3**

**3C** Design a 4- bit ring counter sequences
a)Using D flip-flops;
b) Using Universal shift register IC 74LS194 (universal shift register) **5**

**4A** Design a divide-by-six counter using IC 74LS90 (mod 10 counter). **2**

**4B** A Mealy state machine has a single control input x and the clock, and two outputs A and B. On consecutive rising edges of the clock, the code on A and B changes from 00 to 01 to 10 to 11 and repeats itself if x=1; if at any time, x=0, it holds to the present state, retaining the previous output. Design the state machine using D flip flops. **5**

**4C** An elevator controller takes a 2 bit input that represents the "floor request" FR as shown in table Q 12.1. The controller also generates two output signals to control the "Up and Down movement" of the elevator as shown in table Q 12.2.

Table Q12. 1

| FR1 | FR0 | Floor Request |
|---|---|---|
| 0 | 0 | No request |
| 0 | 1 | Ground floor |
| 1 | 0 | First floor |
| 1 | 1 | Second floor |

Table Q 12.2

| Up | Down | Elevator movement |
|---|---|---|
| 0 | 0 | No movement |
| 0 | 1 | Down |
| 1 | 0 | Up |
| 1 | 1 | Undefined |

Once a passenger enters a floor request, the input persists until the elevator reaches the desired floor and then the input resets to " No request". Develop an **ASM chart** of the elevator controller with the given specifications. **3**

| | | |
|---|---|---|
| **5A** | Construct the logic, F = (A+B) using CMOS logic families. Use minimum number of transistors. | **2** |
| **5B** | Design a 2-bit binary to gray code converter using PLA. | **3** |
| **5C** | Design Verilog HDL code for a full adder using **gate level modeling** and **behavioral modeling**. Illustrate the difference between the two modeling methods. | **5** |