Question Paper

Exam Date & Time: 23-Jan-2023 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

THIRD SEMESTER B.TECH. MAKEUP EXAMINATIONS, JANUARY 2023

ANALOG ELECTRONIC CIRCUITS [ICE 2151]

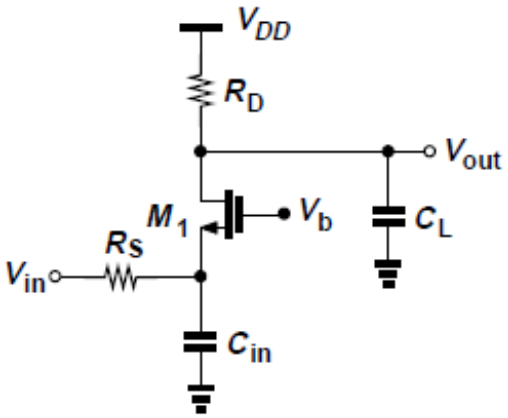
Marks: 50 **Duration: 180 mins.**

A

Answer all the questions.

Instructions to Candidates: Answer ALL questions Missing data may be suitably assumed

1)		An ideal N-channel MOSFET has the following parameters, W = 50 µm, L = 2 µm, μ_n = 450 cm^2/V-sec, t_{ox} = 350 Å and V_{TN} = 0.8 V. If the transistor is biased with gate to source voltage V_{gs} = 4 V and drain to source voltage V_{ds} = 5 V, then evaluate the value of device transconductance. [CO1,BL3, PO2]	(2)
	A)		
	B)	Explain the working of P-channel enhancement type MOSFET in different regions of operations with the help of necessary diagrams. Also, discuss the difference between P-channel enhancement and depletion type MOSFET. [CO1,BL2,PO1]	(4)
	C)	Define the need of source follower stage with suitable example and derive the expression of output impedance for source follower stage with the help of small signal model by considering body effect and channel length modulation parameter λ=0. [CO2, BL3, PO3]	(4)
2)		Compute the voltage gain of common source amplifier with NMOS current source load using small signal analysis. [CO2, BL3, PO2]	(2)
	A)		
	B)	Derive an expression of differential gain for simple MOS differential pair using superposition method ($\lambda_1 = \lambda_2$=0). Also, describe the effect of resistor mismatch on common mode response of the MOS differential pair. [C03, BL3, PO4]	(4)
	C)	Explain the high-frequency model of MOSFET with suitable diagram. [CO3, BL2, PO3]	(4)
3)		What do you mean by frequency response? Why is frequency response important? [CO3, BL2, PO3].	(2)
	A)		
	B)	Compute the poles of the circuit shown below, [CO3, BL3, PO3].	(3)



C) Find the output impedance of the source follower using Miller's approximation. [CO3, BL4, PO3] (5)

4) Show how the linearity can be improved using negative feedback system. [CO4, BL2, PO3] (2)

A)

B) Draw the block diagram of any three feedback topologies. [CO4, BL1, PO3] (3)

C) Determine the closed-loop gain, input and output impedances of the voltage-current feedback topology and analyse the effect of feedback on the input and output impedances. [CO4, BL4, PO3] (5)

5) With suitable circuit diagram derive the expression of differential gain for PMOS current source load based MOS differential pair. [CO2, BL3, PO3] (2)

A)

B) Calculate the efficiency of Class B power amplifier for supply voltage of 24 V, with peak output voltage V_L (p) = 22 V, and also calculate the efficiency of transformer coupled Class A amplifier for a supply voltage of 12 V with output voltage V(p) = 12 V. [CO5, BL3, PO2] (3)

C) With neat circuit diagram explain the operation of FET based Hartley and phase-shift oscillators. [CO5, BL3, PO1] (5)

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