Question Paper

Exam Date & Time: 01-Feb-2023 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

DIGITAL ELECTRONICS CIRCUITS [ICE 2152]

Marks: 50 **Duration: 180 mins.**

Descriptive Questions

Answer all the questions. Section Duration: 180 mins

1) Realize XOR function using NOR gates. Mention any two advantages and two limitations of digital systems in comparison with analog systems. (5)

A) (CO1, PO1, BL2)

B) Design a circuit using minimal SOP form, to detect the decimal numbers 0,1,4,6,7,8 in a 4 bit Excess-3 code. (3)

(CO2, PO3, BL3)

C) Implement the following function using an 8:1 multiplexer: (2)

F(a,b,c) =Σm (0,2,3,5).

(CO2, PO2, BL3)

2) Design a counter using J-K flipflops that goes through the states 3,4,6,7 continuously. Test the counter for self- starting. (5)

A) (CO3, PO3,BL3)

B) Explain the difference between asynchronous and synchronous inputs in a JK flipflop. Explain how the flip flop responds when these inputs are set and reset. (3)

(CO3, PO2, BL4)

C) Given the logic expression Y=A'C+AB', design a hazard free combinational circuit. (2)

(CO2,PO1 ,BL3)

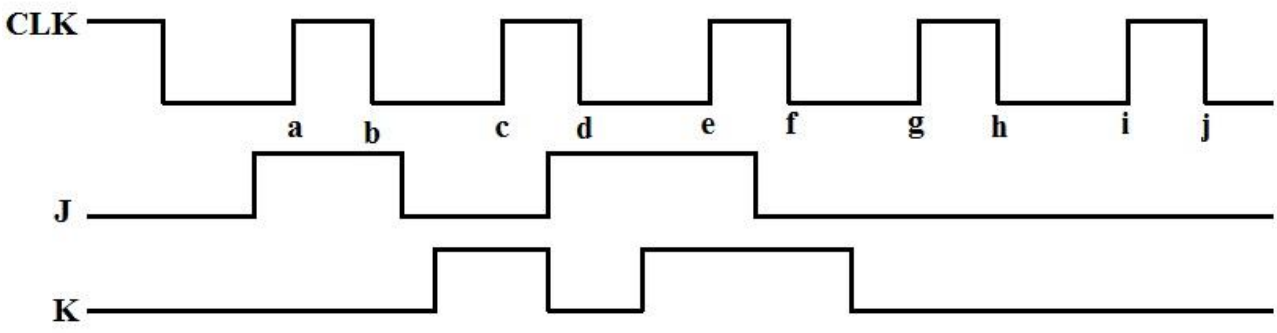
3) How many flip flops are required to design a binary ripple counter that counts up to 16,383 (decimal)? What is the frequency at the output of this counter if the clock frequency is 8.192 MHz? Design a 2-bit asynchronous up counter using negative edge triggered JK flip flops. (5)

A) (CO3, PO3, BL3)

B) Define the components of ASM chart with appropriate representations. (3)

(CO5, PO1, BL2)

C) The waveforms shown in figure are applied to a positive edge and negative edge triggered J-K flip flop. Draw the output waveform in each case. Initially the flip flop is RESET. (2)

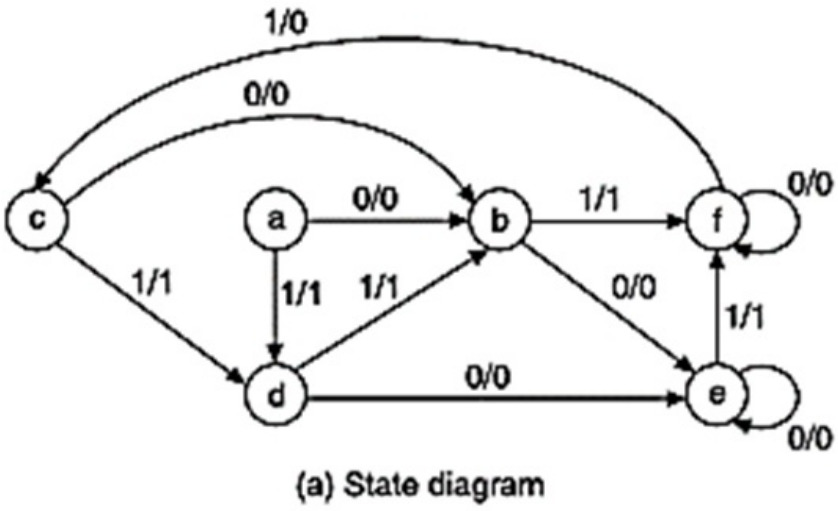


(CO3, PO3, BL3)

4) Explain the working of the shift register counter circuits with the help of suitable block diagrams. (4)

A) (CO4, PO1, BL2)

B) Obtain the reduced state table and the reduced state diagram for the sequence machine whose state diagram is shown below. (3)



(a) State diagram

(CO5, PO3, BL3)

C) Draw the state diagram and ASM chart for a Mod 6 up counter. (3)
(CO5,PO3,BL3)

5) A clocked sequential circuit with single input x and single output z produces an output (5)

A) z = 1 whenever the input x completes the sequence 1110 and overlapping is allowed. Obtain the state diagram and design the circuit with T flip flops for a Mealy type sequence detector. (CO5, PO4, BL4)

B) What do you mean by race conditions in asynchronous sequential circuits? Explain the different types of race conditions using suitable examples. (3)

(CO4, PO3, BL3)

C) Write any two differences between Mealy and Moore type of sequential circuit models. (2)

(CO5, PO1, BL2)

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