Question Paper

Exam Date & Time: 16-Dec-2022 (02:30 PM - 05:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

III Semester End Semester Examination
Digital Electronic Circuits (ICE2152)

DIGITAL ELECTRONICS CIRCUITS [ICE 2152]

Marks: 50 **Duration: 180 mins.**

Descriptive Questions

Answer all the questions. Section Duration: 180 mins

1) Reduce the expression f=A[B+ C' (AB+AC')'] using Boolean algebra and draw the logic diagram using logic gates for the reduced expression. Calculate the percentage reduction in the number of gates required to implement the circuit. Highlight any four advantages of digital systems in comparison with analog systems. (5)

A)

(CO1, PO1, BL2)

B) Using the AND OR INVERTER logic, design a circuit that outputs a 1 when the input is a 4-bit hexadecimal odd number from 0 to 9. (3)

(CO2, PO3, BL3)

C) Implement the following function using a 4:1 multiplexer: (2)

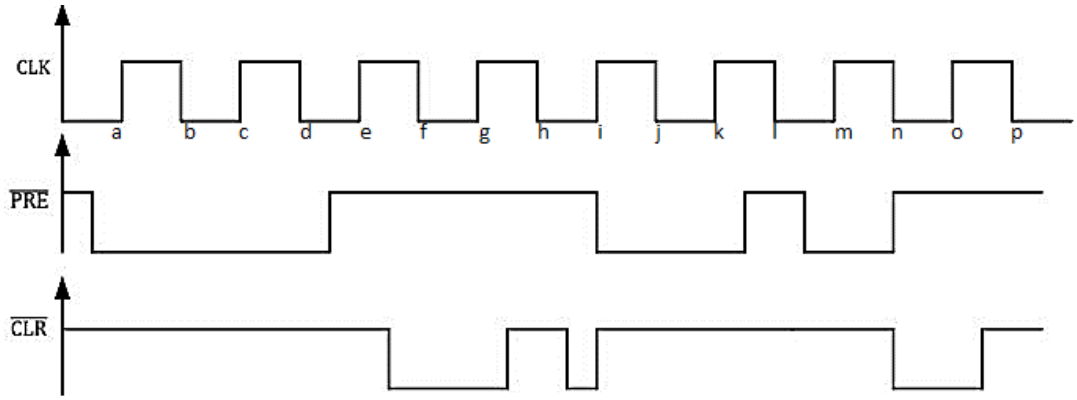
F(a,b,c) =Σm (1,3,5,6).

(CO2, PO2, BL3)

2) Design a synchronous mod-6 counter using J-K flipflops. Test the counter for self- starting. (5)

A) (CO3, PO3,BL3)

B) The waveforms shown in the figure are applied to a positive edge triggered and to a negative edge triggered J-K flip flop. Draw the output waveforms in both the cases assuming J = K = 1. Assume the flip flop is initially reset (Q = 0). (3)



(CO3, PO2, BL4)

C) Given the logic expression Y=AB+B'C, design a hazard free combinational circuit. (2)
(CO2,PO1 ,BL3)

3) Draw the block diagram of a synchronous sequential circuit. Obtain the logic diagram to convert a given D flip-flop to function as a J-K flipflop. (5)

A) (CO3, PO3, BL3)

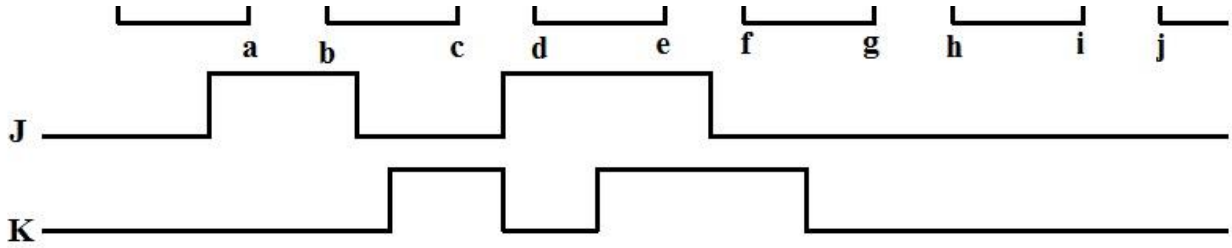
B) An asynchronous sequential circuit is described by the following excitation and output functions. (3)

$$Y = x_1\overline{x_2} + (x_1 + \overline{x_2})y\,;z = y$$

Draw the logic diagram of the circuit. Obtain the output map and the transition table.

(CO4, PO4 / PO3, BL4)

C) The waveforms shown in figure are applied to a master slave J-K flip flop. Draw the output waveform of the slave. Initially the flip flop is RESET. (2)

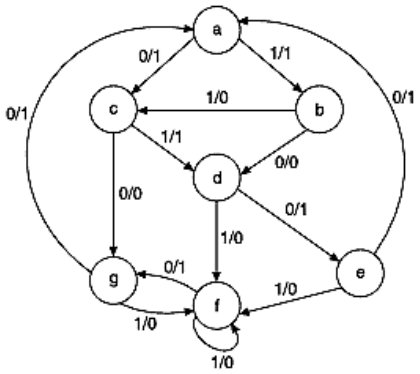


(CO3, PO3, BL3)

4) Explain the working of parallel in serial out and parallel in parallel out shift register circuits with an example and using suitable block diagrams. (4)

A) (CO4, PO1, BL2)

B) Obtain the reduced state table and the reduced state diagram for the sequence machine whose state diagram is shown in figure below. (3)



(CO5, PO3, BL3)

C) Draw an ASM chart and state table for a 2-bit up-down counter having the mode control input M, M = 1 for Up counting and M = 0 for Down counting. The circuit should generate an output '1' whenever the count becomes minimum or maximum. (3)

(CO5, PO3, BL3)

5) A clocked sequential circuit with a single input x and a single output z produces an output z = 1 whenever the input x completes the sequence 1101 and overlapping is allowed. Obtain the state diagram and design the circuit with D flip flops for a Moore type sequence detector. (5)

A) (CO5, PO4, BL4)

B) Define the components of ASM chart with appropriate representations. (3)

(CO5, PO1, BL2)

C) Write any two differences between Mealy and Moore sequential circuit models. (2)

(CO5, PO1, BL2)

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