Question Paper

Exam Date & Time: 13-Dec-2022 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

DEPARTMENT OF INFORMATION AND COMMUNICATION TECHNOLOGY,
THIRD SEM B. TECH (COMPUTER AND COMMUNICATION ENGG.)

DIGITAL SYSTEMS AND COMPUTER ORGANIZATION [ICT 2171]

Marks: 50 **Duration: 180 mins.**

A

Answer all the questions.

Instructions to Candidates: Missing data may be suitably assumed

1)		Write the advantages and limitations of carry propagation adder, carry look ahead adder and carry save adder. Illustrate the working of all these three methods for adding four 4-bit numbers: $(1001)_2$, $(1110)_2$, $(1100)_2$, $(1101)_2$.	(5)
	A)		
	B)	Design an asynchronous UP counter to count from $(2)_{10}$ to $(6)_{10}$ using positive edge triggered D - flip flops and minimum external gates.	(3)
	C)	Design T - flip flop using NOR latch and external gates.	(2)
2)		Design a sequence detector with one input Y and one output Z. The output Z is HIGH whenever the sequence "1001" is detected, otherwise the output is LOW. Overlapping of the sequence is allowed. Implement using JK- flip flops and minimum number of external gates.	(5)
	A)		
	B)	A Computer system has a 128 K of main memory and 4K of cache memory. The cache block size is 8 words. Calculate the tag field width for fully associative mapping, direct mapping and 4-way set associative mapping schemes.	(3)
	C)	Design a combinational circuit that compares two, 4 - bit numbers to check if they are equal using logic gates. The circuit output is equal to 1, if the two numbers are equal and 0 otherwise.	(2)
3)		Design a code converter to convert a decimal digit represented in 8 4 2 1 code to a decimal digit represented in gray code using basic gates.	(5)
	A)		
	B)	Why is non restoring division algorithm more efficient than restoring division algorithm? Divide $(10101)_2$ by $(110)_2$ using non restoring division algorithm. Show all the steps.	(3)
	C)	Using asynchronous decade counter ICs and external gates, design a 2 - digit decimal counter which counts from $(00)_{10}$ to $(86)_{10}$ and repeats.	(2)
4)		With a suitable design, explain the two different control unit design techniques? Mention their merits and demerits.	(5)
	A)		
	B)	Using ring counter, generate the sequence 01011. Use JK flip flops and minimum external gates for the design.	(3)

C) Design a 4:2 priority encoder and realize the circuit using basic gates. (2)

5) Design a self-correcting synchronous counter using T - flip flops and minimum number of external gates to count the sequence 1 → 3 → 2 → 5 → 4 →1 when control input Y=0 and count the sequence 1 → 4 → 5 → 2 → 3 →1 when control input Y=1. The undefined count should restart the counter from count 1 during the next clock. (5)

A)

B) With the help of neat diagram, explain various techniques to handle multiple interrupts. (3)

C) Design a 4-bit combinational shifter to function according to the Table Q.5C. (2)

Table Q. 5C

Control input	**Output**
00	Parallel load
01	Rotate left once
10	Rotate left twice
11	Rotate left thrice

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