Question Paper

Exam Date & Time: 23-Jan-2023 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

DEPARTMENT OF INFORMATION AND COMMUNICATION TECHNOLOGY,
THIRD SEM B. TECH (COMPUTER AND COMMUNICATION ENGG.) MAKE UP EXAMINATIONS

DIGITAL SYSTEMS AND COMPUTER ORGANIZATION [ICT 2171]

Marks: 50 **Duration: 180 mins.**

A

Answer all the questions.

Instructions to Candidates: Missing data may be suitably assumed

1)		Draw the flowchart of booths multiplication algorithm. Perform the multiplication of $(15)_{10}$ by $(7)_{10}$ using the same algorithm indicating all the steps.	(5)
	A)		
	B)	Design an asynchronous 4 - bit UP/ DOWN counter using negative edge triggered JK - flip flops and minimum 2:1 multiplexer.	(3)
	C)	Design D - flip flop using NAND latch and external gates.	(2)
2)		Design a sequence detector with one input Y and one output Z. The output Z is HIGH whenever the sequence "1011" is detected, otherwise the output is LOW. Overlapping of the sequence is allowed. Implement using JK- flip flops and minimum number of external gates.	(5)
	A)		
	B)	With the help of a neat diagram, explain microprogrammed control unit design.	(3)
	C)	Design a combinational circuit that compares two, 2 - bit numbers to check if A>=B using logic gates. The circuit output is equal to 1, if the two numbers satisfy the condition A>=B.	(2)
3)		Design a code converter to convert a decimal digit represented in gray code to a decimal digit represented in excess-3 code using 3:8 decoders and minimum external gates.	(5)
	A)		
	B)	What is Direct Memory Access (DMA)? Explain the three different DMA data transfer techniques.	(3)
	C)	Using a synchronous hexadecimal counter ICs and external gates, design a 2 - digit hexadecimal counter which counts from 23 H to 56 H and repeats.	(2)
4)		Write the importance of cache mapping techniques. With the help of neat diagrams, explain the three cache mapping techniques.	(5)
	A)		
	B)	Using Johnson counter, generate the sequence 00011001. Use JK flip flops and minimum external gates for the design.	(3)
	C)	Explain the pros and cons of booths multiplication algorithm over add and shift method.	(2)
5)		Design a self - correcting synchronous UP counter to count in 8 4 2 1 code using T - flip flops and minimum number of external gates. The undefined count should restart the counter from count 0	(5)

A) during the next clock.

B) Design a binary multiplier to multiply two, unsigned 3- bit numbers using minimum external gates and 7483 ICs. (3)

C) Carry save addition is faster that carry propagation addition (True/False). Justify. (2)

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