Question Paper

Exam Date & Time: 13-Dec-2022 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

THIRD SEMESTER B.TECH. (INFORMATION TECHNOLOGY) EXAMINATIONS - DECEMBER 2022
SUBJECT : ICT 2154 - DIGITAL SYSTEMS

Marks: 50 **Duration: 180 mins.**

Answer all the questions.

1A)	Design a combinational circuit to perform F= A-B when control input Y=0 and perform F= 1+2A-B when control input Y=1 using 4 - bit parallel binary adders and minimum universal gates. Assume A, B and F are 4 - bit binary numbers.	(5)
1B)	Design an asynchronous Down counter to count from 5 to 2 using positive edge triggered D - flip flops and minimum external gates.	(3)
1C)	Design T - flip flop using NAND latch and external gates.	(2)
2A)	Design a sequence detector using Mealy model with one input Y and one output Z. The output Z is HIGH whenever the sequence "1001" is detected, otherwise the output is LOW. Overlapping of the sequence is allowed. Implement using JK- flip flops and minimum number of external gates.	(5)
2B)	Realize the Boolean functions: $F_1(A,B,C) = \sum_m (0,1,2,5)$ and $F_2(A,B,C) = \prod_M (1,5,6)$	(3)
2C)	Design a combinational circuit that compares two, 4 - bit numbers to check if they are equal using logic gates. The circuit output is equal to 1, if the two numbers are equal and 0 otherwise.	(2)
3A)	Design a code converter to convert a decimal digit represented in 8 4 -2 -1 code to a decimal digit represented in gray code using 3:8 decoders and minimum external gates.	(5)
3B)	Design a 16: 1 MUX using 2: 1 MUXs ONLY.	(3)
3C)	Using asynchronous hexadecimal counter ICs and external gates, design a 2 - digit hexadecimal counter which counts from 00 to 89H and repeats.	(2)
4A)	Minimize the following using Qunie McCluskey Method $F(A, B, C, D) = \Sigma m\ (4,5,6,8,10,13)$ and realize using basic gates.	(5)
4B)	Design sequence generator using johnson counter (shift register) to generate sequence 1101.	(3)
4C)	Design a 4 x 16 decoder using only 3 x 8 decoders.	(2)
5A)	Design and implement a MOD-5 synchronous counter using JK flip-flops and draw its timing diagram.	(5)
5B)	Design a 2X2 bit combinational multiplier using basic gates.	(3)
5C)	Solve the POS function minimization of 5 variable K-Map using the following expression: πM(0,2,4,7,8,10,12,16,18,20,23,24,25,26,27,28).	(2)

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