Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

DEPARTMENT OF MECHATRONICS ENGINEERING

III SEMESTER B.TECH. (MECHATRONICS)

END SEMESTER EXAMINATIONS, December 2022

SUBJECT: DIGITAL SYSTEM DESIGN [MTE 2152]

10/12/2022

Time: 3 Hours **MAX. MARKS: 50**

Instructions to Candidates:

- Answer **ALL** the questions.

Q. No		M	CO	PO	LO	BL
1A.	Implement the given function $f(A,B,C,D)=\bar{A}\bar{D}+\bar{C}\bar{D}+A\bar{C}D+AC\bar{D}$. i. Using only NAND gates. ii. Using only NOR gates.	**4**	**1**	**1, 3**	**1, 2, 3**	**3**
1B.	Obtain a minimal SOP expression using QM method for the following equation. $F(A,B,C,D)=\sum m(1,2,3,4,10,11,12,14)+d(5,15)$	**4**	**1**	**1, 3**	**1, 2, 3**	**3**
1C.	Using 74283 develop a 4 bit Binary to Excess 3 code converter	**2**	**2**	**1, 3**	**1, 2, 3, 5**	**3**
2A.	Implement the four Boolean functions listed below using three half adder circuits. $D=A\oplus B\oplus C$ $E=\bar{A}BC+A\bar{B}C$ $F=AB\bar{C}+(\bar{A}+\bar{B})C$ $G=ABC$	**4**	**2**	**1, 3**	**1, 2, 3**	**3**
2B.	Implement full subtractor using 2 to 4 decoder and residual gates	**3**	**2**	**1, 3**	**1, 2, 3, 5**	**3**
2C.	A mux-based circuit is given in the **Fig. 2C**. Analyze the circuit and find the expression of Z0, Z1 and Z2 .	**3**	**2**	**1, 2**	**1, 2, 3**	**3**

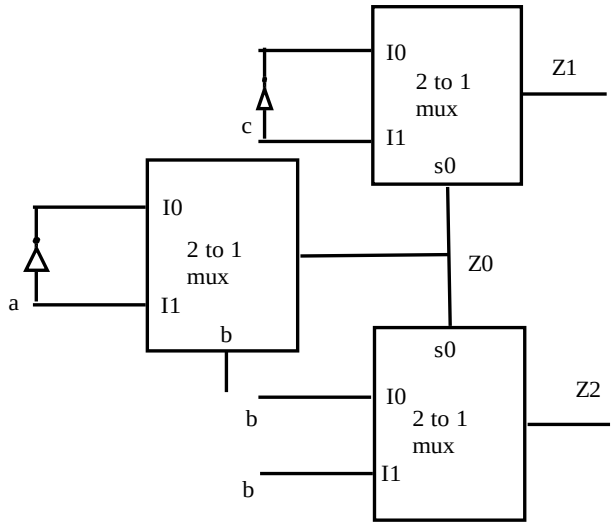

Fig. 2C

3A.	A shift register needs to be designed to perform the following operations. Design a suitable circuit. **S1** / **S0** / **Operation** 0 / 0 / Shift left 0 / 1 / Shift right 1 / 0 / Synchronous preset 1 / 1 / Hold	**5**	**3**	**1, 2**	**1, 2, 5**	**6**
3B.	Implement the following equations using PLA. $F_1 = ABC + A\bar{B}\bar{C}$ $F_2 = AB + BC + CA$	**3**	**4**	**1, 6**	**3, 7, 8**	**3**
3C.	Is FPGA better compared to Semi Custom and Full Custom ASIC. Support your argument with a suitable explanation and example	**2**	**4**	**1, 2, 4**	**2, 4, 7**	**5**
4A.	The chocolate making company uses cocoa beans to make chocolate. The beans are initially roasted using heater for definite time and then, it is cooled down to decrease the temperature for few seconds. Assume that there are 4 cocoa beans. The process must start with loading of beans to a heater. The beans are loaded sequentially indicated by "1111". The beans get heated immediately and will be available at the output of the heater at 4s. After this process, the heater should automatically turn off and based on the switch, the cocoa beans should be loaded into a cooler. Once the cooling process starts, the temperature of the beans will be reduced to a certain level and will be available at the output after 7s. The entire process of increasing and decreasing the temperature should finish at 11s. The block diagram of the same is shown in **Fig. 4A**. Design a suitable circuit with minimal components. (Clearly state if any assumptions are made)	**5**	**3**	**1, 2, 3**	**1, 2, 3, 5**	**6**

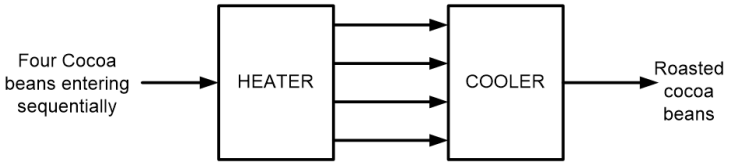

Fig. 4A

4B.	Design a 4 bit Fibonacci counter using T flipflop that counts the sequence starting from 0001 till 1101 and then repeats from 0001.	**3**	**3**	**1, 2, 3**	**1, 2, 3, 5**	**6**
4C.	Design an asynchronous counter that counts from 3 to 9 and then restarts from 3.	**2**	**3**	**1, 2, 3**	**1, 2, 3, 5**	**3**
5A.	Design a sequence generator using IC74194 for the sequence 0,8,12,6,13,11,7,3,1,0……	**4**	**3**	**1, 2, 3**	**1, 2, 3, 5**	**6**
5B.	Write a Verilog code along with expected output for the problem statement mentioned. A sequential circuit has eight states that are coded into three bits in binary counting order. Besides clock, the machine has 2 inputs, reset, and enable and one output "done". The machine should go to state 0 whenever reset is asserted. When reset is negated, it should move to the next number only if the enable is asserted. However, once it reaches 8^{th} state, it should stay there unless the reset is again asserted. The done output should be high if and only if the machine is in 8^{th} state and enable is asserted. (State the assumptions clearly in case if any)	**4**	**5**	**1, 2, 3**	**1, 2, 3, 5**	**6**
5C.	Write a Verilog code to implement a 4:16 decoder using 2:4 decoder only	**2**	**5**	**1, 2, 3**	**1, 2, 3, 5**	**6**