Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FIFTH SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION
NOVEMBER 2022
SUBJECT: MICROPROCESSORS (ECE - 3153)

TIME: 3 HOURS **MAX. MARKS: 50**

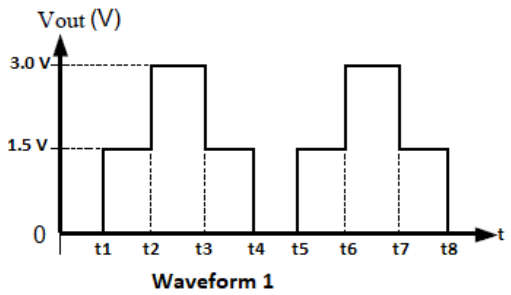
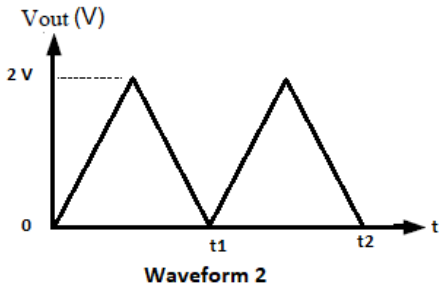
Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

Q. No.	Questions	M*	C*	A*	B*

1A	For the following code, how many clock cycles are required to complete the execution of all instructions, in a 3-staged pipelined processor? Draw the pipeline diagram for the same. Justify how the performance of this pipelined processor is improved as compared to a non-pipelined processor.
	AREA PROG1, CODE, READONLY
	ENTRY
	MOV R2, #76
	MOV R3, #8
	B UP
	ADDS R1, R2, R3
	CMP R1, #0XFF
	MOVNE R4,#0
	UP SUB R1, R2, R3
	EOR R3,R3,R3
	END
		4	1	1,2,18	3

1B	Differentiate between CISC and RISC architecture. Describe how ARM architectural features are enhanced from RISC architecture.	3	1	1,2,18	2
1C	Describe the privileged operating modes of ARM7TDMI processor. With the help of a neat diagram, show the banked registers for each mode.	3	1	1,2,18	2
2A	Explain the function of following ARM7 instructions in detail and also rewrite the content of all the affected registers and memory locations after execution each of the instruction. Assume the same PRE condition for each instruction.: R0=0x40000000, R1=0x1A2B3C4D, R2=0x98765432, R3=0x55994422, R4=0x12345678	4	2	1,2,3, 4,18	3

Memory address	32-bit value
0x40000000	0xAABBCCDD
0x40000004	0xEEFF6789
0x40000008	0x12344321

	i. BIC R4, R1, R2 ii. STRB R1, [R0, R2, LSR #29]! iii. RSB R3, R2, R4 iv. SWPB R2, R3, [R0]				
2B	Describe all the single-register load/store addressing modes of ARM7 processor for half-word/signed half-word/signed byte operation.	3	2	1,2,3, 4,18	2
2C	Identify the correct instructions of ARM7 for the following 32-bit binary code and also justify your answer with relevant explanation: i. 0xE0810312 (hint: Data processing instruction) ii. 0xE7943245 (hint: Data transfer instruction)	3	2	1,2,3, 4,18	3
3A	Write an Assembly Language program in ARM 7 to check whether the given 16-bit number is prime or not. If the given 16-bit number is prime store "0x1111" in the memory otherwise "0xFFFF".	4	2	1,2,3, 4,18	4
3B	Explain the features of following functional blocks of LPC2148. i. Watchdog timer ii. Pulse width modulator	3	3	1,4,6, 18	2
3C	Explain the following Assembler directives of ARM with an example for each i. AREA ii. EXPORT iii. FILL	3	2	1,2,3, 4,18	2
4A	Explain the following registers of LPC2148 with neat bit structure: i. DACR ii. ADxCR	4	3	1,4,6, 18	2
4B	Describe the nested interrupt handler scheme used in ARM7 processor, with the help of a diagram.	3	4	1,3,4, 18	2
4C	With the help of an example and pipelining diagram, explain how the value in link register is adjusted while handling an IRQ exception in ARM7.	3	4	1,3,4, 18	2
5A	Interface two switches (SW0 and SW1) to LPC2148 microcontroller through P0.6-P0.7 port lines of PORT0 respectively. Write an embedded C program to generate the waveforms using internal DAC as per the given condition. i. If SW0 is closed, generate waveform 1 ii. If SW1 is closed, generate waveform 2  Waveform 1  Waveform 2	4	3	1,4,6, 18	4
5B	Write a C program for OMAP L138 to generate a sinusoidal signal of 3 kHz without using lookup table. Filter the generated sinusoidal signal using a moving average filter.	3	5	1,2,4, 18	3

5C	Write a C program to create a fading echo effect on the input audio signal using OMAP L138. Assume that only 50% of the output signal is fed back to the input.	3	5	1,2,4, 18	3

M*--Marks, C*--CLO, A*--AHEP LO, B* Blooms Taxonomy Level