Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FIRST SEMESTER M.TECH. (POWER ELECTRONICS & DRIVES)

END SEMESTER EXAMINATIONS, JANUARY 2023

EMBEDDED SYSTEM DESIGN [ELE 5171]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 10 January 2023** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. An optimal processor is to be selected among two general purpose processors for an application which mainly involves integer arithmetic and string operations. Suggest and describe a suitable benchmark to select the processor. ***(03)***

1B. i. List the main features and specifications of PIC16F877 microcontroller.

ii. Explain the following PIC16F877 instructions. Illustrate with an example.

a. MOVWF f

b. ADDLW K ***(04)***

1C. Answer the following with respect to undefined instruction exception.

i. When does this exception occur?

ii. What is the main reason for having this exception in APM7TDMI?

iii. What is the expected operation in the undefined exception handler?

iv. Mention and describe the instruction used to return from undefined exception handler. ***(03)***

2A. A programmer uses MOV PC, LR instruction of ARM7 to return from all the subroutines in case of nested subroutine. Illustrate with an example, the problem with this approach. Suggest and illustrate a method to overcome this problem and to return correctly. ***(03)***

2B. Write equivalent ARM7 assembly program for the following 'C' code.

```
while (a!=b)
{
  if (a>b)
  a = a-b;
  else
  b = b-a;
}
```

Mention the mathematical operation performed by this code. Illustrate the same by taking a suitable example. ***(03)***

2C. Design an interfacing circuit to interface two common cathode 7-segment LED display devices to mbedNXPLPC1768 microcontroller. Use GPIO pins p10 to p17 and p20 to p27 for the interface. Write a 'C' program to display numbers '00' to '99' continuously on the display devices with a delay of 3.45 sec between each display. ***(04)***

3A. Analyze and determine the best cache design among the following (based on the average cache access time). System clock frequency is 500MHz.

i. In a system with single cache (L1 cache only) out of 6000 attempts to access memory, there are 750 cache misses.

ii. In a system with two levels of cache (L1 and L2 cache) out of 9000 attempts to access memory, there are 2000 misses in L1 cache, 600 misses in L2 cache. ***(03)***

3B. With the help of a relevant block diagram, describe the compromise protocol for read operation. Compare the protocol with strobe and handshake protocols and highlight the relative merits and demerits. ***(03)***

3C. Develop a 'C' program for PIC16F877 microcontroller to configure the MSSP in SPI master mode to transmit data bytes 3AH and 4BH to slave device-1 connected to RB1 pin and data bytes 2CH and 1AH to slave device-2 connected to RB2 pin at 1.25 Mbps baud rate. Use idle state for clock as high level, transmit data on falling edge, sample input data at the end of data output time. Consider f_{osc} = 20MHz. ***(04)***

4A. Describe the protocol used by CAN serial communication bus for data transfer. Explain in detail all the fields involved in the data transfer and hence differentiate between remote frame and data frame. ***(03)***

4B. i. The Positive and negative reference voltages of ADC in PIC16F877 are '5' V and '0' V respectively. If an analog voltage input of 3.6V is converted to digital, determine the values of ADRESH and ADRESL registers (with left justified result format).

ii. Develop a 'C' program to convert the analog input applied to RE0 / AN5 pin of PIC16F877 microcontroller and display the result at ports 'B' and 'D'. Use right justified result, conversion time of 24μs, positive and negative reference voltages from V_{DD} and V_{SS} pins. All the remaining pins of ports A and E should be available as analog input pins. Assume f_{osc} = 1MHz. ***(04)***

4C. Develop a pseudocode to realize the ATM timeout using watchdog timer and explain the operation. ***(03)***

5A. Describe in brief the various stages involved in the design of an embedded system ***(04)***

5B. Three peripherals P1, P2, and P3 are to be connected to a processor in daisy chain arbitration scheme. It is found that P2, and P3 are daisy chain aware and P1 is not daisy chain compatible. Design a suitable logic circuit to make P1 daisy chain compatible. Do not modify the priority of the devices. Illustrate the working of the designed logic circuit. ***(03)***

5C. In a chemical plant following three real time tasks are to be scheduled on a uniprocessor.

Task-1: Monitor the temperature value every 5s. Worst case processing time for temperature is 1s.

Task-2: Monitor the humidity value every 6s. Worst case processing time for humidity is 1.9s.

Task-3: Monitor the pressure value every 18s. Worst case processing time for pressure is 3.5s.

Determine the total task utilization time by the processor and develop a suitable schedule to schedule these tasks using Rate monotonic algorithm for one hyper period. ***(03)***