MANIPAL INSTITUTE OF TECHNOLOGY
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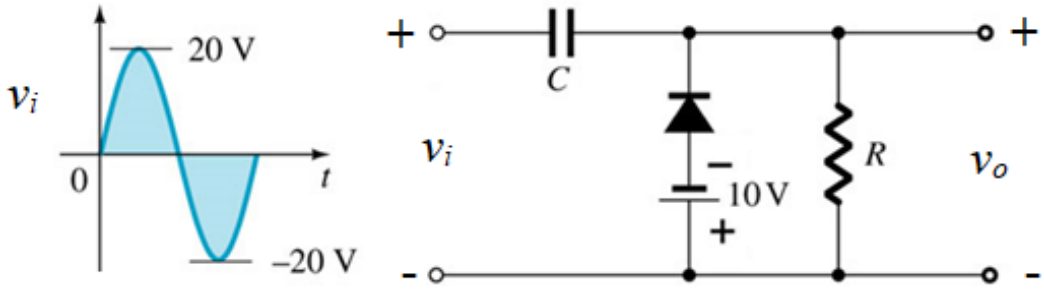
DEAPRTMENT OF MECHATRONICS
I SEMESTER M. TECH (INDUSTRIAL AUTOMATION AND ROBOTICS)
END-SEMESTER EXAMINATION – JANUARY 2023

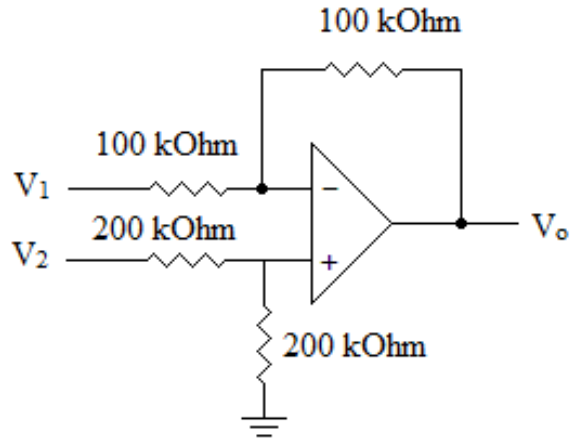
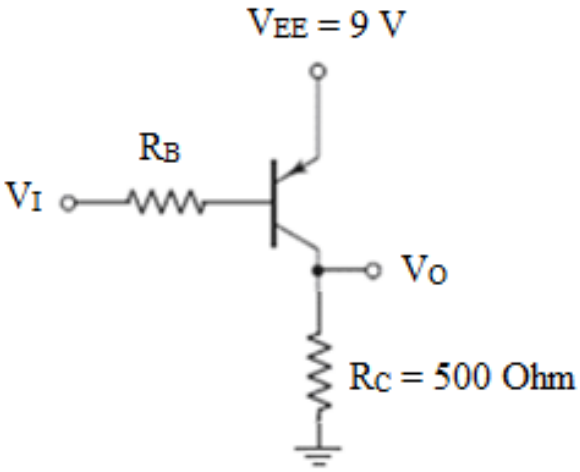
Subject: Analog and Digital Electronics (PE-1) **Subject Code: MTE 5001**

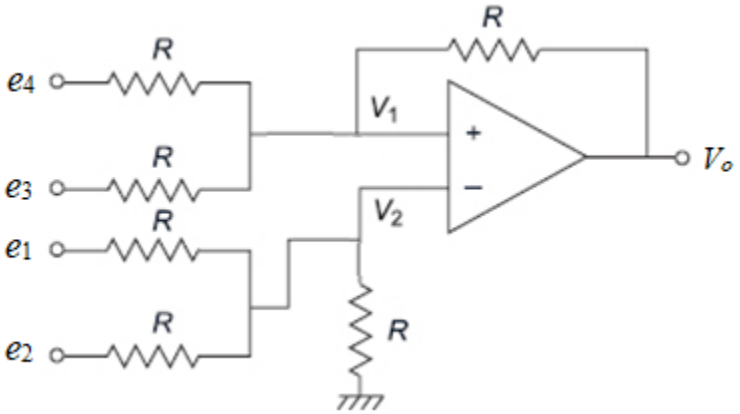
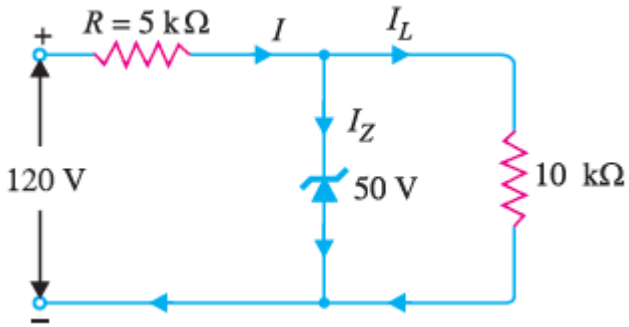
Time: 3 hours **Exam Date & Time: 5th Jan. 2023; 9:30 AM to 12:30 AM** **Max. Marks: 50**

Instructions to Candidates:

- ***Answer ALL the questions.***
- *Missing data may be suitably assumed and justified.*
- *For problems, digital and analog circuit with appropriate symbols may be given.*
- *Write your Name, Registration Number, Roll Number at top of every page of the answer sheet.*

Q. No.	Problem Statement	M	CO	LO	PO	BL
Q1A.	Construct the circuit to realize the below given output voltage using one op-amp and passive components: $V_o = -2V_1 + V_2 + 2V_3$ where V_1, V_2 and V_3 are the input voltages.	**05**	**4**	**1**	**4**	**6**
Q1B.	Analyse the circuit given in **FIG. 1B** showing equivalent circuit. Plot the output waveform assuming ideal diode. Identify the circuit with justification.  **FIG. 1B**	**03**	**3**	**1, 2**	**4**	**4**
Q1C.	Determine the output voltage of an op-amp based circuit in **FIG. 1C** when V_1 = 1 V and V_2 = -1 V.	**02**	**4**	**1**	**4**	**5**

	 **FIG. 1C**					
Q2A	The turns ratio of a transformer used in a Full-wave Bridge Rectifier is 12:1. The primary of transformer is connected to the power mains 220 V, 50 Hz. Neglecting diode voltage drops, (a) find the DC voltage across load resistor, (b) what is the PIV of the diode? (c) if the same dc voltage is obtained by using center tapped full-wave rectifier, what is the PIV?	**05**	**3**	**1,2**	**4**	**3**
Q2B.	Given that the dc load line cuts the x-axis and y-axis of output characteristics of BJT at 20 V and 8 mA respectively. Given that I_B = 40 μA and β = 50, design a fixed bias circuit. Find the value of operating point.	**03**	**3**	**1,2**	**4**	**6**
Q2C.	The current gain β for the transistor in the circuit shown in **FIG. 2C** is 25. Determine R_B such that $V_o = 8.8$ V when $V_I = 5$ V.  **FIG. 2C**	**02**	**3**	**2**	**4**	**3**
Q3A.	Consider both 4-bit binary code and 4-bit gray code (let the gray code be reflective with respect to LSB). Solve for 4-bit Binary-to-Gray code converter logic circuit considering the K-map. Give the logic circuit implementation of same.	**05**	**1**	**2**	**4**	**6**
Q3B.	For the circuit in **FIG. 3B**, determine the expression for V_o.	**03**	**4**	**1,2**	**3,4**	**5**

	 **FIG. 3B**					
Q3C.	Compare BJT and FET with respect to following parameters: (i) Input control, (ii) Temperature sensitivity, (iii) Input impedance (for CE, CS)	**02**	**3**	**3**	**4**	**2**
Q4A.	[i] For the circuit shown in **FIG. 4A,** find the following: a) the output voltage b) the voltage drop across series resistance **c)** the current through Zener diode.  **FIG. 4A** [ii] Show how ± 5 V voltage regulator can be designed using 3 terminal IC voltage regulators.	**05**	**3,5**	**1,2**	**4**	**3**
Q4B.	Draw the circuit of 4-bit binary weighted resistor DAC. Given that $V_{ref} = 8$ V. Compute the following: (a) Resolution in voltage. (b) Full-scale output voltage. (c) Output voltage V_o for digital input $b_3b_2b_1b_0 = 0011$	**03**	**3**	**2**	**4**	**3**
Q4C.	Why 2's complement is considered better than 1's complement? Illustrate with an example.	**02**	**1**	**2**	**4**	**2**

Q5A.	[i] A logic circuit has 3 inputs and 1 output variable. The output is at logic 1 when two or more inputs are at logic 1. Write the truth table. Simplify the SOP expression using Boolean algebra and realize using NAND gates. Comment on the logic circuit. [ii] Build the optimal realization of half-subtractor using only (a) NAND gates, (b) NOR gates. Compare number of NAND/ NOR gates required.	**05**	**1**	**2**	**4**	**3**
Q5B.	Construct 4-bit PISO shift register using JK flip-flops and asynchronous parallel-load feature. Explain the working of the same.	**03**	**2**	**2**	**4**	**6**
Q5C.	Construct the logic circuit for a 4-bit ripple counter using D flip-flop. Given the time period of the output waveform of last flip-flop is 64 µs. Find the frequency of clock used.	**02**	**2**	**2**	**4**	**3**