

# Question Paper

Exam Date & Time: 09-Jan-2023 (10:00 AM - 01:00 PM)



## MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal  
First Semester Master of Engineering - ME (Embedded Systems) Degree Examination - January 2023

### Advanced Computer Architecture [ESD 5101]

Marks: 100

Duration: 180 mins.

Monday, January 9, 2023

Answer all the questions.

- 1) Describe Von-Neumann and Harvard architecture machines and Compare (TLO 1.1 - CO1) (10)
- 2) Illustrate the implementation of a 4-bit carry propagate adder. Model a 16-bit adder using the above 4-bit adder and calculate the computation time. (TLO 2.2 - CO2) (10)
- 3) Illustrate Non-restoring algorithm to perform the division of two unsigned numbers: Dividend: 14 and Divisor: 3 (TLO 2.3 - CO2) (10)
- 4) Illustrate 4x4 Combinational Shifter and show the hardware that can rotate left a 16-bit data by 0, 1, 2 or 3 positions. (TLO 2.1 - CO2) (10)
- 5) **Devise hardware to implement each of the following register transfers:** (10)

a) If X is even                      then  $A \leftarrow B \text{ OR } C$   
   else  $A \leftarrow (B \text{ AND } C)'$

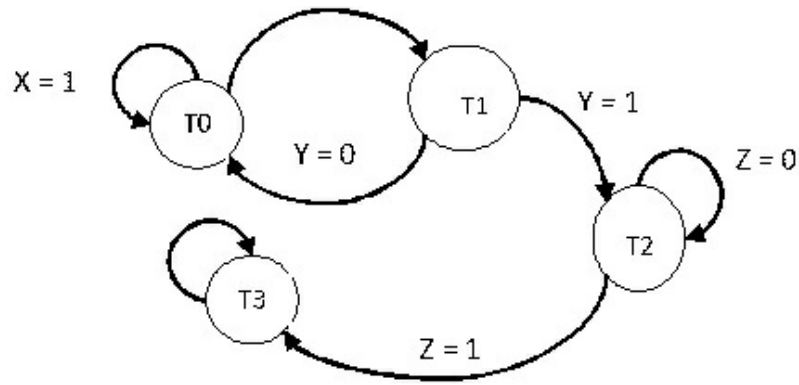
b) If X is zero                      then  $A \leftarrow A \text{ plus } 1$   
   else  $A \leftarrow A \text{ minus } 1$

Assume that A, B, C and X are 4 – bit registers. (TLO 3.3 – CO3)

- 6) (10)

A control circuit has three inputs X, Y & Z and its state diagram is shown below. Design the control circuit using counter, decoder and PLA (TLO 3.3 – CO3)

X = 0



- 7) Describe Endianness and explain two types of data stored in memory with an example. Explain three types of index addressing modes with an example for each (TLO 3.1 - CO1) (10)
- 8) Discuss the need of memory mapping function, describe 3 types of memory mapping function with page replacement policies. (TLO 4.2 - CO1) (10)
- 9) Write a note on pipelining in a single processor system and its advantages, illustrate a four-stage single instruction pipeline. (TLO 5.1 - CO3) (10)
- 10) Describe the following parallel computing taxonomy: (10)  
(a) SISD (b) SIMD (c) MISD (d) MIMD (TLO 6.1 - CO1)

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