Question Paper

Exam Date & Time: 11-Jan-2023 (02:00 PM - 05:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
First Semester Master of Engineering - ME (Embedded Systems) Degree Examination - January 2023

System on Chip Design [VLS 5132]

Marks: 100 **Duration: 180 mins.**

Wednesday, January 11, 2023

Answer all the questions.

1) Define is instruction level parallelism (ILP)? How Very long instruction word (VLIW) processors exploit ILPs? Explain by comparing with simple sequential processors with the help of an example. (10)

(TLO - 1.1)

2) Explain hardware/software co-design space. (10)

(TLO - 1.4)

3) Explain briefly about post-partitioning analysis and debug in ESL flow (10)

(TLO - 2.3)

4) Explain four design principles in SoC with suitable examples (10)

(TLO - 3.1)

5) What are the types of branch prediction? Explain bimodal and two-level adaptive predictions (10)

(TLO - 4.4)

6) State the dependencies in instructions shown below. Show and describe the timing for a dataflow with three separate floating-point unit and single floating-point instructions. The adder unit, multiply unit and divider unit takes 2, 4 and 6 clock cycles to complete their operations respectively. (10)

ADD R4, R3, R8
MUL R8, R3, R1
DIV R3, R2, R1

(TLO - 4.5)

7) Define Transaction Lookaside Buffer. Explain the address translation with the help of a neat block diagram. (10)
Determine the average access time assuming a TLB hit ration of 0.85 with the following specification
Number of entries in the TLB = 16
Time taken to conduct an associative search in the TLB = 100 ns
Main memory access time = 1.1 us

(TLO - 5.1)

8) Explain the three types of cache organization with neat diagrams (10)

(TLO - 5.3)

9) Give the structure of AMBA bus-based system in a System on Chip. Explain the simple AMBA High performance Bus transfers with neat diagrams (10)

(TLO - 6.2)

10) Describe the various dimensions of the synchronization problems in Hardware-Software Interfaces (10)

(TLO - 7.1)

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