Question Paper

Exam Date & Time: 11-Jan-2023 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
First Semester Master of Engineering - ME (VLSI Design) Degree Examination - January 2023

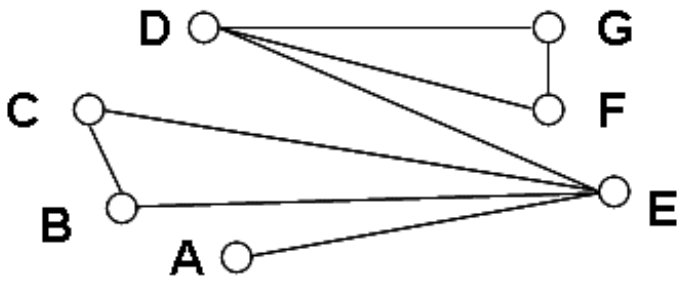
CAD for VLSI (Elective-1) [VLS 5131]

Marks: 100 **Duration: 180 mins.**

Wednesday, January 11, 2023

Answer all the questions.

1)	Describe the various entities for optimization in VLSI design. [TLO 1.1]	(10)
2)	Explain the different steps and tools in Structural and Logic Design. [TLO 2.1]	(10)
3)	Discuss the following. [TLO 2.1] a) Logic synthesis (5) b) Transistor level design (5)	(10)
4)	Illustrate and expalin the hierarchical clustering algorithm with an example. [TLO 4.1]	(10)
5)	Describe how loops are scheduled. [TLO 4.2]	(10)
6)	Using the clique partitioning algorithm, partition the following graph. [TLO 4.2]	(10)



7)	Explain floor planning in physical design. Illustrate the floor plan based design methodology and list its merits. (3+7) [TLO 5.1]	(10)
8)	a) Explain the terms: i) Routing ii) Local routing iii) Global routing (6) [TLO 6.1] b) Describe any four parameters that affect routing. (4)	(10)
9)	Illustrate Lee's algorithm for area routing with an example. [TLO 6.1]	(10)
10)	Explain the longest path algorithm for directed acyclic graphs with an example. [TLO 7.1]	(10)

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