Question Paper

Exam Date & Time: 06-Jan-2023 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
First Semester Master of Engineering - ME (VLSI Design) Degree Examination - January 2023

Verification [VLS 5103]

Marks: 100 **Duration: 180 mins.**

Friday, January 6, 2023

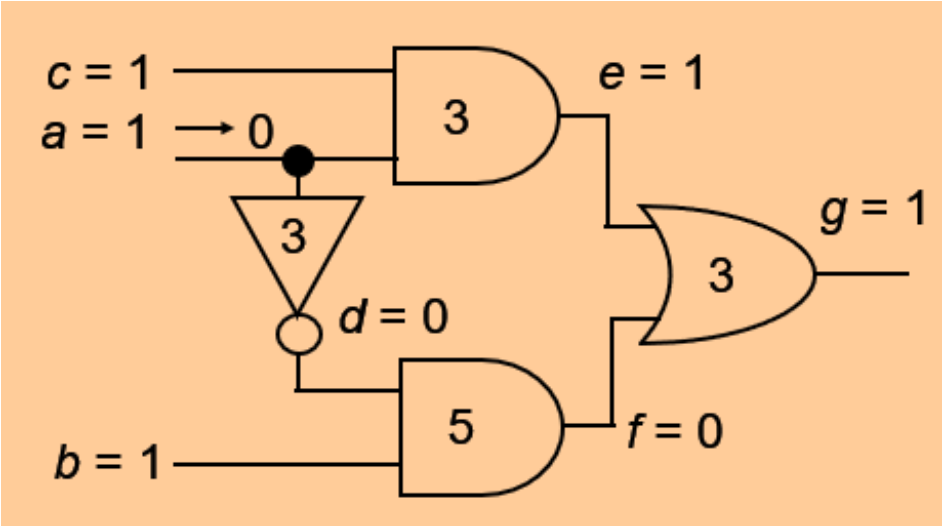
Answer all the questions.

1) Describe verification challenges with respect to Missed bugs, Lack of Time, and Lack of resources. Explain the significance of modified V approach in verification with suitable examples. (10)

(TLO -1.1)

2) Describe event driven and cycle-based simulation. List out the scheduled events and activity list for the given circuit. Provide the timing diagram for the output *g*. (10)

(TLO -2.2)



3) Explain block coverage and branch coverage with suitable examples (10)

(TLO -2.3)

4) Give a general structure of testbench in verification environment. List and explain any 5 general rules in testbench architecture. (10)

(TLO - 5.4)

5) Describe the possible ways of applying reset to a design and mention which approach would be better. (10)

(TLO - 6.2)

6) Mention the advantage of self-checking testbenches. Give a self-checking testbench for a BCD counter with active high synchronous reset. Assume a carry signal HIGH when counter reaches maximum value. (10)

(TLO - 6.3)

7) Explain functional coverage modeling and functional coverage implementation. (10)

(TLO - 7.2)

8) Describe model checking and assertions in verification process with suitable examples (10)

(TLO - 8.1)

9) Describe the process of verifying transaction-level models with a neat block diagram and example (10)

(TLO - 9.3)

10) Describe pre-silicon and post-silicon validation process (10)

(TLO - 11.1)

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