Question Paper

Exam Date & Time: 29-May-2023 (02:30 PM - 05:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

FOURTH SEMESTER B.TECH END SEMESTER EXAMINATIONS, MAY 2023

DIGITAL SYSTEM DESIGN [BME 2253]

Marks: 50 **Duration: 180 mins.**

A

Answer all the questions.

Instructions to Candidates: Answer ALL questions Missing data may be suitably assumed

1) Solve using minimum CMOS transistor network that implements the functionality of Boolean equation **Y = A . (B + C) + CD** (4)

A)

B) Explain with a neat diagram the structure of ***Standard cell*** (4)

C) Identify any two differences between ***Full custom*** and ***Semi custom design*** (2)

2) Design a 2:1 MUX with the help of block diagram and corresponding truth table using pull up and pull down transistors (4)

A)

B) Design a 2:1 MUX with the help of Shannon's expansion theorem for the given function (4)

$$F = \overline{w1}\ \overline{w3} + w1w2 + w1w3$$

C) Deduce the given Boolean function using CMOS TX gate (2)

$$F = AB + \overline{A}\overline{C} + A\overline{B}C$$

3) Solve the following function using ***PAL*** (4)

A) $f1 = x1\ x2\ \overline{x3} + \overline{x1}\ x2\ x3$ $and\ f2 = \overline{x1}\ \overline{x2}$ ***+ x1 x2 x3***

B) Solve the following function using ***PLA*** (4)

$$f1 = x1\ x2 + x1\ \overline{x3} + \overline{x1}\ \overline{x2}\ x3$$

$$and\ f2 = x1x2 + \overline{x1}\ \overline{x2}\ x3 + x1\ x3$$

C) Generalize any two differences between PLA and PAL (2)

4) Design a JK Flip flop with the relevant circuit using ***Gate level Verilog code*** (4)

A)

	B)	Design a SR Flip flop with the relevant circuit using ***Data Flow Verilog code***	(4)
	C)	Design a half adder with the relevant circuit using ***Gate level Verilog code***	(2)
5)		Design ***CMOS SR Latch using NAND gates*** with a) Circuit diagram of SR Latch b) Truth table of SR Latch c) Pull up and pull down circuit.	(5)
	A)		
	B)	Summarize any three differences between ***CPLD*** and ***FPGA***.	(3)
	C)	Explain Moore's law with the corresponding diagram	(2)

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