Exam Date & Time: 06-Jul-2023 (02:30 PM - 05:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

FIRST SEMESTER B.TECH END SEMESTER MAKEUP EXAMINATIONS, JUNE-JULY 2023

DIGITAL SYSTEM DESIGN [BME 2253]

Marks: 50 **Duration: 180 mins.**

A

Answer all the questions.

Instructions to Candidates: Answer ALL questions Missing data may be suitably assumed

1) Solve using minimum CMOS transistor network that implements the functionality of

A) Boolean equation $F= ((A+B)\ C + D)'$ (4)

B) Explain with the neat diagram structure of ***Gate Array*** (4)

C) Identify any two differences between ***Full custom*** and ***Semi custom design*** (2)

2) Design a two input CMOS NOR gate with the help of neat circuit and corresponding truth table considering the details of pull up and pull down transistors. (4)

A)

B) Design a 4:1 MUX with the help of Shannon's expansion theorem for the given function

$F = \overline{w1}\ \overline{w3} + w1w2 + w1w3$ (4)

C) Deduce the given Boolean function using CMOS TX gate

$F= A\overline{B} + \overline{A}\ B$ (2)

3) Solve the following function using ***PLA***

A) $A= XY + X\overline{Z}$

$B = X\overline{Y} + YZ + X\overline{Z}$ (4)

B) Solve the following function using ***PAL*** (4)

$$F1 = \sum m(3, 5, 7)$$

$$F2 = \sum m(4, 5, 7)$$

C) Write any two differences between PLA and PAL (2)

4) Design a JK Flip flop with the relevant circuit using ***Data Flow Verilog code.*** (4)

A)

B) Design a SR Flip flop with the relevant circuit using ***Gate Level Verilog code.*** (4)

C) Design a half adder with the relevant circuit using ***Data Flow Verilog code.*** (2)

5) Design ***CMOS SR Latch using NOR gates*** with a) Circuit diagram of SR Latch b) Truth table of SR Latch c) Pull up and pull down circuit. (5)

A)

B) Identify any three differences between ***CPLD*** and ***FPGA.*** (3)

C) Write any two advantages of VLSI technology. (2)

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