Question Paper

Exam Date & Time: 22-May-2023 (02:30 PM - 05:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

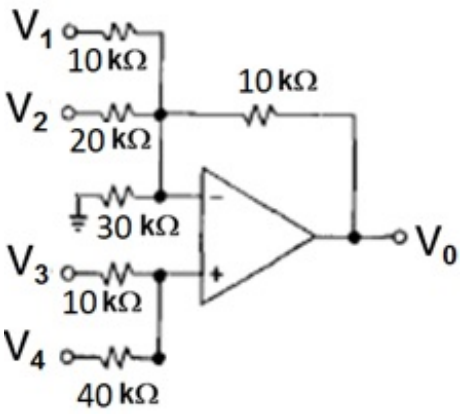
FOURTH SEMESTER B.TECH. (ELECTRONICS AND COMMUNICATION ENGINEERING) EXAMINATIONS - MAY/JUNE 2023
SUBJECT: ECE 2253/ ECE_2253 - LINEAR INTEGRATED CIRCUITS

Marks: 50 **Duration: 180 mins.**

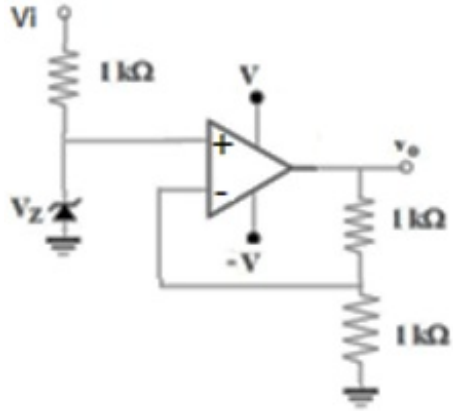
Answer all the questions.

Missing data may be suitably assumed.
Assume Opamp saturation voltage to be ±12V.

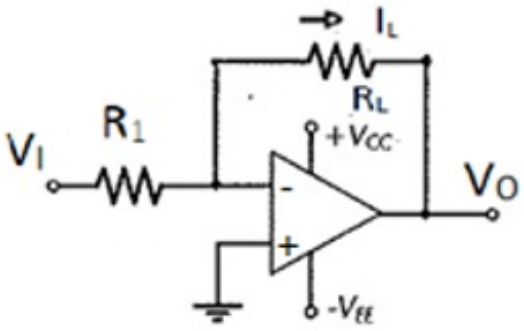
1A) Obtain expression for output voltage of the circuit shown below. Also if V_1 is varied from 0 to 10 V, keeping V_2, V_3,V_4 at 1V, sketch output voltage with respect to input voltage. (5)



1B) In the Circuit shown in figure, an ideal Zener diode with breakdown voltage of 4.7V is used. Plot the output voltage verses the input voltage. Input voltage varies from 0 to 15 V. (3)



1C) Circuit shown below is voltage to current converter. Given V_I = 2 V , R_1 = 1 kΩ maximum output current through the op-amp is ±10 mA. Determine (i) I_L (ii) Maximum value of R_L that can be used. (iii) Maximum value of V_I that can be used, given R_I = 1kΩ and R_L = 0. (2)



2A) Design a Butterworth LPF with cut-off frequency, f_c = 1kHz for the frequency response shown in Fig. Q2A. (5)

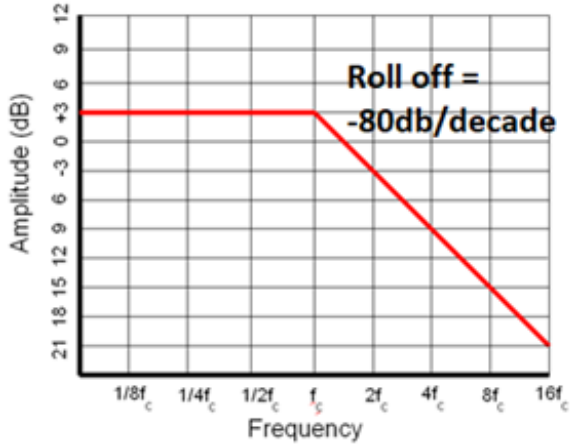


Fig. Q2A

2B) Analyse the temperature compensated logarithmic amplifier with a neat diagram and obtain the output expression. (3)

2C) For the circuit shown in Fig. Q2C. given a silicon diode, and V_{Sat} = ±13V. Draw the transfer characteristics. (2)

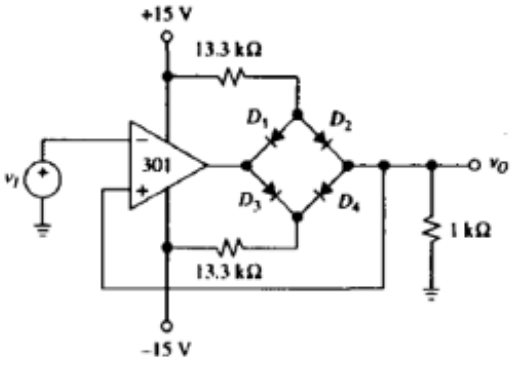
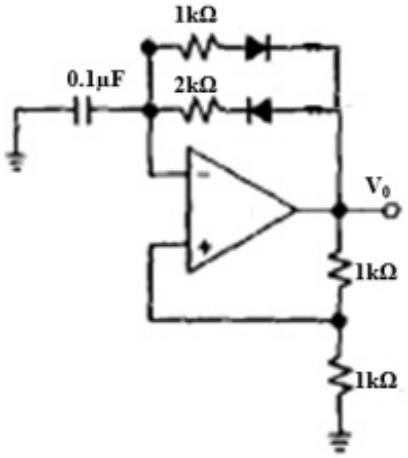


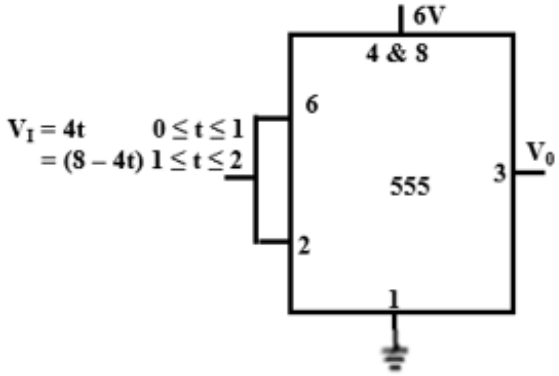
Fig. Q2C

3A) i) By marking all the voltage levels and time intervals, plot V_0 as a function of time for the circuit shown in figure. (5)
ii) What would be the effect on waveform, if 2kΩ resistor is replaced by a 1kΩ fixed resistor in series with a 1kΩ potentiometer and the latter is varied from minimum to maximum value.



3B) Design a 555 timer based circuit to give a square waveform of 1kHz frequency and duty cycle adjustable between 25% to 75%. (3)

3C) For the circuit of shown, if V_I is a triangular waveform defined as in figure, by marking all the time intervals and voltage levels, plot V_0 as a function of time. (2)



4A) Design a astable multivibrator shown in Fig. Q4A having with frequency 1KHz. Assume C = 0.1μF, also find the duty cycle D. (5)

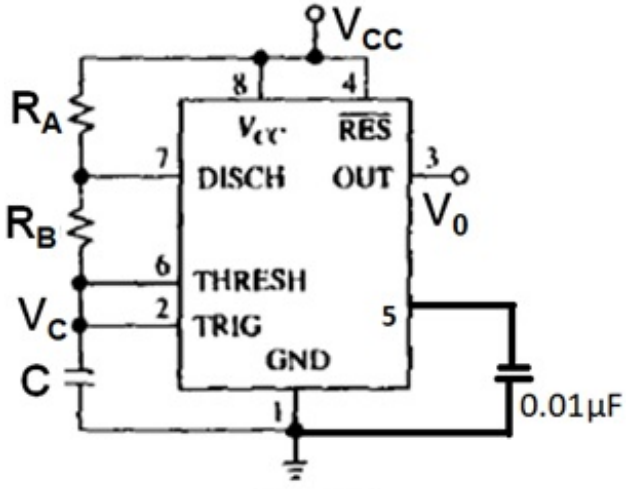


Fig. Q4A

4B) Draw the internal diagram of VCO and explain its working. (3)

4C) With a neat block diagram explain the working of frequency multiplier using PLL. (2)

5A) Design a 4-bit R - 2R DAC to result in an output voltage of 0.5V when the input is 0001. Use V_{REF} of -5V and resistor connected to output terminal of 1kΩ value. What would be the output voltage when the input is 1111. Plot V_0 if the input is coming from a 4-bit Johnson counter driven with a 1kHz clock signal. (5)

5B) Explain the working principle of a SAR ADC with an example. (3)

5C) In a 4 bit ADC, if the clock frequency is 1kHz, determine the minimum and maximum conversion (2)

time, if the ADC is (i) counter type (ii) successive approximation type.

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