Question Paper

Exam Date & Time: 31-May-2023 (02:30 PM - 05:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

FOURTH SEMESTER B.TECH. (ELECTRONICS AND COMMUNICATION ENGINEERING) DEGREE EXAMINATIONS - MAY/JUNE 2023
SUBJECT: ECE 2254/ECE_2254 - VLSI DESIGN

Marks: 50 **Duration: 180 mins.**

Answer all the questions.

Missing data may be suitably assumed.

1A) Discuss the operation of any two different forms of pull-up for an NMOS inverter circuit. Draw transfer characteristics for these different forms of pull-up. Compare the relative merits of these different forms of pull-up. (4)

1B) With neat diagrams, explain the working of the MOS capacitor. Briefly illustrate the fabrication steps of a MOS Capacitor. (3)

1C) Refer the pass-transistor based logic network given in **FIG 1C**. (3)
(a) Determine the truth table for the circuit and indicate the logic function performed by the topology?
(b) Specify the role of PMOS transistor in this circuit?

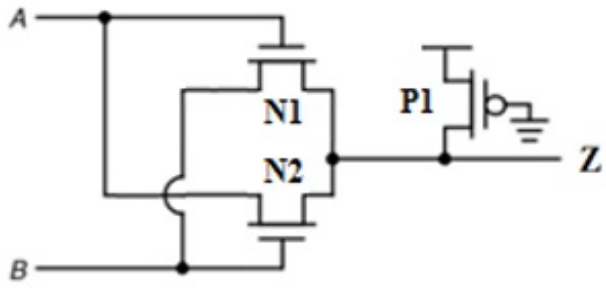


Fig. 1C

2A) Implement Static CMOS circuit of half Adder with truth table. (4)

2B) Implement and explain the working of 2 input NOR using clocked CMOS(C²MOS) and draw the stick diagram. (3)

2C) Explain with diagram, the working of 4X4 OR ROM for the table given and draw Stick diagram. (3)

word	BL[1]	BL[2]	BL[3]	BL[4]
W[1]	1	0	0	1
W[2]	0	1	1	0
W[3]	1	0	1	1
W[4]	1	1	0	1

3A) Sketch the layout of a CMOS 3-input NAND gate using λ-based design rules. Use either colour code/ shades as per the standard conventions to distinguish different regions/layers. (4)

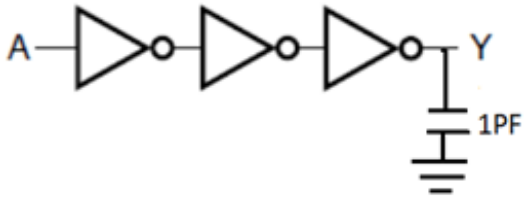
3B) A semi-conductor industry wants to fabricate a MOS with its substrate as pentavalent impurities and (3)

trivalent impurities as source and drain. Explain the steps involved in the fabrication of the mentioned MOS.

3C) List the steps involved Fin-FET fabrication process with neat diagrams. (3)

4A) Implement an static CMOS circuit of Y=(A+B+C)| and Draw the layout. (4)

4B) Calculate the total delay in geometrically cascaded CMOS inverters shown in the figure below. Assume f=e=2. 7==3. (3)



4C) Derive the scaling factors with respect to MOSFET. (3)
i) Gate Area
ii) Gate capacitance per unit Area
iii) Gate capacitance

5A) Construct a CMOS PLA to implement the following functions (4)
X = AB′D + A′C′ + BC + C′D′
Y = A′C′ + AC + C′D′
Z = CD + A′C′ + AB′D

5B) Demonstrate how the basic building block of an Arithmetic Logic Unit (ALU) can be employed to implement a 2-input logic OR function. (3)

5C) Illustrate a 1-bit right shift operation on the input word '0010' using Barrel shifter and provide its circuit diagram. (3)

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