Question Paper

Exam Date & Time: 24-May-2023 (02:30 PM - 05:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

FOURTH SEMESTER B.TECH END SEMESTER EXAMINATIONS, MAY 2023

DIGITAL SYSTEM DESIGN [ICE 2251]

Marks: 50 **Duration: 180 mins.**

A

Answer all the questions.

Instructions to Candidates: Answer ALL questions Missing data may be suitably assumed

1) Distinguish between top-down and bottom-up design methodology with an example of a 4-Bit ripple carry counter.[CO2, PO1,2,3,12, BL2] (3)

A)

B) Use structural modelling technique to implement a full adder using two half adders. [CO3, PO1,2,3, BL3] (4)

C) Based on the choice of the system user, one of the following four options is implemented, model the system using dataflow method and write a brief note explaining your logic. [CO3, PO2,3, BL3] (3)

Option	Action
1	Rotate half step Clockwise (CW)
2	Rotate half step Counter Clockwise (CCW)
3	Rotate full step Clockwise (CW)
4	Rotate full step Counter Clockwise (CCW)

2) Differentiate among any four different programming technologies that are used to make the FPGAs field programmable. [CO4, PO2,3, BL2] (4)

A)

B) Given inputs are: a = 4'b1010, b = 4'b1111. What would be the output in the following cases? (4)

i. a & b ii) a && b iii) & a iv) a >> 1

v. a >>> 1 vi) y = {2{a}} vii) a ^ b viii) z = {a, b}

[CO3, PO1,3,12, BL3]

C) What is the difference between the following two lines of Verilog code? (2)

#5 a = b;

a = #5 b; [CO3, PO1,2,3, BL3]

3) Implement a synchronous machine in Verilog that detects two successive bursts of logic 1 followed by two successive bursts of logic 0. Draw a timing diagram for the same, showing inputs, state transitions, and sequence detection. [CO3, PO1,2,3,12, BL4] (5)

A)

B) Write a Verilog code that implements the following operation depending on the input select S1 and S0. Given A and B are 4 bit inputs. (3)

S1	S0	Operation
0	0	1's complement of A
0	1	2's complement of B
1	0	reversing the bit position of A
1	1	reversing the bit position of B

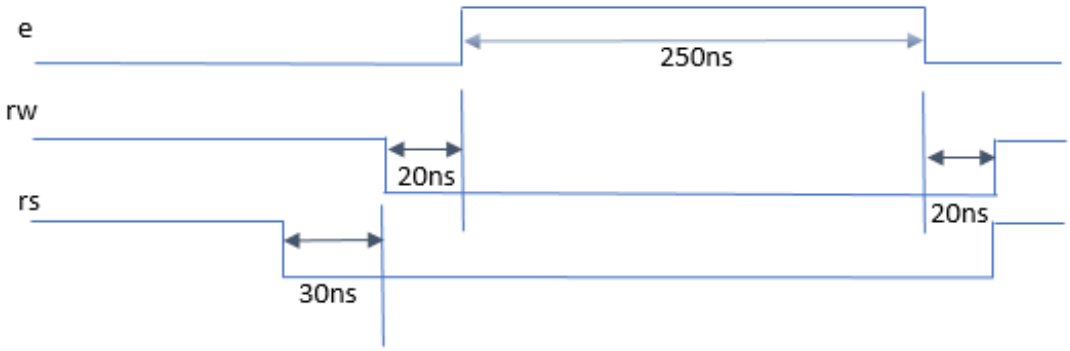
[CO3, PO1,2,12, BL3]

C) Differentiate between tasks and functions in Verilog. [CO4, PO1,2,3,12, BL2] (2)

4) Draw a neat block diagram of a Mealy machine. [CO3, PO1,2,3,12, BL2] (2)

A)

B) Design a digital system to generate the following waveform. Assume a system clock with period 10ns. [CO3, PO1,2,3,12, BL4] (5)



C) Implement a UDP for a level-sensitive latch with clear. [CO3, PO1,2, BL3] (3)

5) Compare sequential and parallel blocks with appropriate examples. [CO4, PO1,3, BL3] (3)

A)

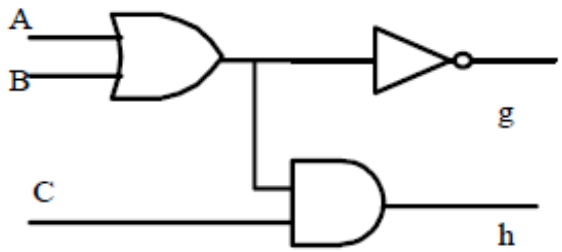
B) A full subtractor has three 1-bit inputs, x, y, and z (previous borrow), and two 1-bit outputs D(Difference) and B(Borrow). The logic equations are: (4)

$$D = \bar{x}\bar{y}z + \bar{x}\,y\bar{z} + x\bar{y}\bar{z} + xyz$$

$$B = \bar{x}y + \bar{x}z + yz$$

Write Verilog description using dataflow modeling. Instantiate the subtractor module inside a stimulus block and test all possible combinations of inputs x, y, and z. [CO4, PO1,2, BL3]

C) Develop the test vectors to test the logic circuit below for all stuck at faults. [CO5, PO1,2,12 BL4] (3)



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