Question Paper

Exam Date & Time: 29-May-2023 (02:30 PM - 05:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

FOURTH SEMESTER B.TECH END SEMESTER EXAMINATIONS, ICE, MAY 2023

LINEAR INTEGRATED CIRCUITS [ICE 2254]

Marks: 50 **Duration: 180 mins.**

A

Answer all the questions.

Instructions to Candidates: Missing data may be suitably assumed

1) Illustrate the effect of resistance mismatches for a difference amplifier. Obtain the expression for common mode rejection ratio considering the mismatch. [CO1, PO4, BL3] (3)

A)

B) Differentiate the sourcing and sinking current flow directions for inverting and non-inverting amplifier circuits for an input voltage $V_i < 0V$ with suitable circuit diagrams [CO1, PO1, BL4] (3)

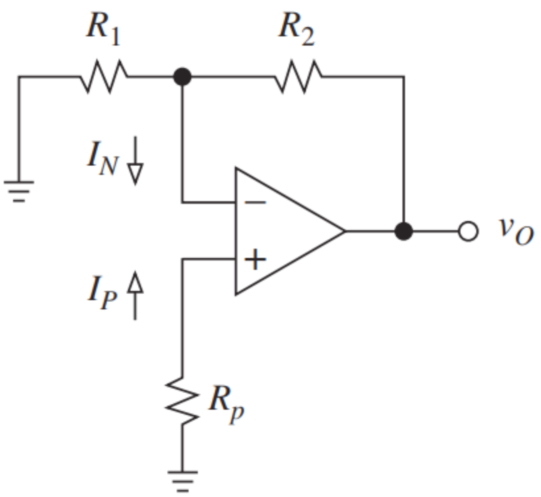
C) Design a 4th order Butterworth low pass filter with cut-off frequency, f_c = 4.5 kHz by considering capacitance of value C = 0.0047 μF and suitable assumptions. Draw the relevant circuit diagram. Normalized Butterworth Polynomial for 4th order filter is $(s^2 + 0.765s + 1)(s^2 + 1.848s + 1)$ [CO2, PO2, BL3] (4)

2) Illustrate Slew rate for μA741 with an example. [CO2, PO2, BL3] (2)

A)

B) In the circuit shown, let R_1 = 12 kΩ and R_2 = 1.2 MΩ, and the op amp ratings be I_B = 80 nA and I_{OS} = 20 nA. (a) Calculate E_O for the case R_p = 0; (b) Calculate E_O for $R_p = R_1 || R_2$; (c) Calculate E_O with all resistances simultaneously reduced by a factor of 10 for $R_p = R_1 || R_2$. (3)

$$E_O = \left(1 + \frac{R_2}{R_1}\right)\{[(R_1 \parallel R_2) - R_p]I_B - [(R_1 \parallel R_2) + R_p]I_{OS}/2\}$$



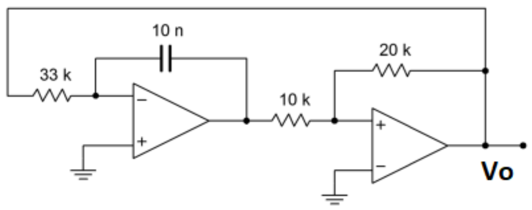
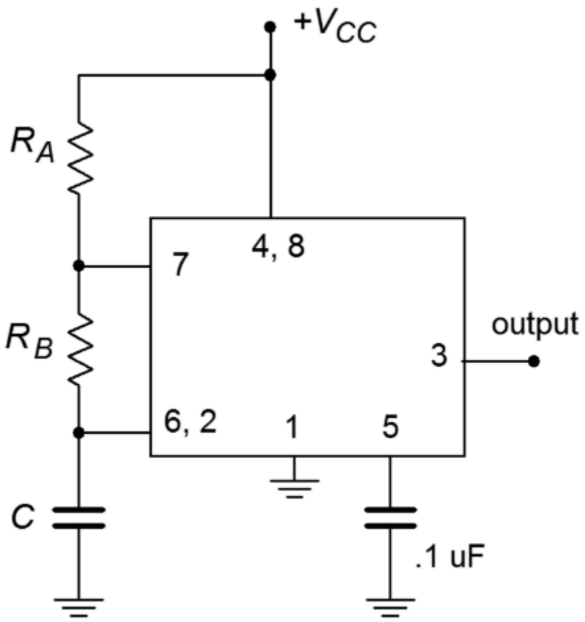
[CO2, PO2, BL3]

C) Arrive at an expression of voltage to frequency conversion factor in a voltage-controlled oscillator. [CO5, PO2, BL3] (5)

3) Explain the different compensation techniques used for nullifying the input offset in operational amplifiers. [CO2, PO1, BL2] (3)

A)

B) Illustrate the track and hold mode of peak detector using op amps with relevant circuit diagrams and waveforms[CO3, PO1, BL3] (4)

C)		With appropriate circuit diagram, design an inverting Schmitt trigger circuit whose upper threshold voltage is +2.5 V and lower threshold voltage is -4 V. Op-amp is powered with ±11V supply. Calculate the Hysteresis voltage. What will be the output waveform if the input voltage is set to $3V_{peak\ to\ peak}$? [CO3, PO3, BL3]	(3)
4)		Determine the output frequency and amplitude at Vo for the given circuit. Use Vsat = ±13 V. [CO3, PO3, BL4]	(3)
A)			
B)		Design a 2KHz square wave generator shown in figure using a 555 timer with 80% duty cycle. [CO3, PO3, BL4]	(4)
			
C)		Discuss the working of Dual-Slope type Analog-Digital Converter (ADC) using suitable block diagram. [CO4, PO2, BL2]	(3)
5)		Describe any one application of Phase locked loop. [CO5, PO2, BL3]	(2)
A)	i		
	ii	The data sheet of the REF101KM 10V precision voltage reference gives a typical line regulation of 0.001%/V, a typical load regulation of 0.001%/mA and a maximum thermal coefficient of 1ppm/°C. Find the variation in Vo brought by a) change of Vi from 13.5 V to 35 V; b) ±10mA change in Io; c) temperature change from 0°C to 70°C. [CO5, PO2, BL3]	(3)
B)		For the 4-bit weighted resistor DAC, determine (a) the weight of each input bit if the inputs are 0V and 5V, (b) the full-scale output, if R_F = R = 1kΩ. Also, (c) find the full-scale output if R_F is changed to 500Ω. [CO4, PO2, BL3]	(3)
C)		List the applications of monostable multivibrator. [CO3, PO1, BL2]	(2)

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