Reg. No.



## VI SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING) END SEMESTER EXAMINATIONS, MAY 2023

## FPGA BASED SYSTEM DESIGN [ELE 4063]

REVISED CREDIT SYSTEM

Time: 3 Hours

## Date: 30 May 2023

Max. Marks: 50

## Instructions to Candidates:

- ✤ Answer ALL the questions.
- Missing data may be suitably assumed.
- **1A** For each of the application mentioned below, examine for the most appropriate implementation option among FPGA, microcontroller, standard cell, and full-custom IC technologies. Provide the explanation for option selected in each case.
  - i. A digital system to control an automatic sliding door at a shop.
  - ii. A hand-held power efficient digital system for signal monitoring applications with short design time.
  - iii. A digital finger-print recognition system for replacing the paper tickets by electronic tickets at a football stadium with large capacity

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**1B** Develop the synthesized circuit for the Verilog code given below: Use multiplication and adder blocks in the circuit for multiplication and addition operations.

```
module digitalcircuit(
output [15:0] Z,
input [15:0] P, Q, R, Y,
input clk,
input samplev);
reg [15:0] Y1, Y2, Z;
reg [15:0] pr1, pr2, pr3;
always @ (posedge clk) begin
if(samplev) begin
Y1 <= Y;
Y2 <= Y1;
pr1 <= P * Y;
pr2 <= 0 * Y1;
pr3 <= R * Y2;
end
Z \le pr1 + pr2 + pr3;
end
endmodule
```

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	the following details.	
	i. ii. iii.	4 numbers of 4 pico second. Carry and contro 2 numbers of multiplexer (F6)
	The imp and min	plemented circuit s nimum delay.
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- should have minimum numbers of CLBs

2:1 multiplexers (F5) and one 2:1

- rol Logic
- m3, m4, m5, m6, and m7) that outputs 1 when motion is detected. Create FPGA based circuit that sounds an alarm if motion is detected in any one of the rooms. The FPGA CLB architecture has the following details input LUT. Each LUT adds a delay of 50
- connects 3 computers together and allows them to send messages to each other. If two or more computers send messages simultaneously, they collide and messages must be resent. Collision detection circuit generates high output if two or more computers send messages simultaneously. **3C** A museum has 8 rooms each with a motion sensor (m0, m1, m2,
- **3A** Explain with sketches dynamic reconfiguration in FPGA to reconfigure the system to adapt dynamically to environmental or operational changes. Explain the features of dynamic reconfiguration. 3B Develop a self-checking Verilog Test-bench code for collision

detection circuit with the following function. A network router

- circuit in FPGAs with least routing delay. Explain with sketches how the connections are made in this technology. **2C** Discuss the benefits of using a soft embedded processor in an

- **2B**
- Choose an appropriate programming technology to implement the
- Mention the assumptions made.
- ADD instruction: Add the data present in two registers iii. and write result back to one of the registers
- ii. Store instruction: Store the data from any register in the

FPGA over a hard-macro implementation?

**1C** 

- register file to any data memory location
- Load instruction: Load the data from data memory to i. one of the registers in register file
- a simple programmable logic device. **2A** for a processor with the following three instructions.
  - Using the RTL design approach develop data-path and control unit

Design a digital system to be used as a patient attendant system

with the following requirements. A patient can push the Call button to turn ON a small green light near nurse reception desk indicating the patient needs help/attention. The light stays ON even after the call button is released. The light can be turned OFF by pressing the **Cancel** button. Implement the digital circuit using

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- **4A** A museum has 4 rooms, each with a motion sensor (m0, m1, m2, and m3) that outputs 1 when motion is detected. After the museum has been closed for the public, the only person in the museum is one security guard walks from room to room. Create FPGA based circuit (FPGA (Partial) architecture is shown in the figure) for the following
  - i. Circuit that sounds an alarm (output is 1) if motion is ever detected in more than one room at a time (meaning there must be an intruder or intruders in the museum).
  - ii. Circuit that detects whether the guard is properly patrolling the museum.

The FPGA architecture has several CLBs and switch matric. CLB consists of a LUT and a D flip flop. LUTs have 3 inputs, and two outputs. Each switch matrix has two numbers of 4 input multiplexers.

Estimate the reconfiguration bit file (LUTs and switch matrix) needed to realize the circuit on FPGA



Figure FPGA (Partial)

**4B** Consider the state diagram shown in Fig.Q5C. Test for the shortest input sequence that will distinguish the state transitions. Also verify all the state transitions from state B and state D.



Fig. Q5C

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**4C** Explain the need for the Delay Locked Loop as one of the reconfigurable blocks in FPGA.

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**5A** Calculate the critical path delay and the frequency of clock required for the digital circuit shown in the Figure. Consider wire delay of 0.5 ns.



- **5B** A network router connects 3 computers together and allows them to send messages to each other. If two or more computers send messages simultaneously, they collide and messages must be resent. Estimate minimum set of test vectors that detect all stuckat-0 and stuck-at-1 faults in the collision detection circuit.
- **5C** Develop FPGA based architecture to implement 4 tap linear phase FIR filter. High speed is one of the constraints. Justify the circuit suitability for high speed applications. Also, estimate the output y[3] using the developed FPGA based architecture if  $h[n]=[\mathbf{3} \ 5 \ 3]$  and  $x[n]=[\mathbf{6} \ 3 \ 2 \ 4]$  where h[0]=3 and x[0]=6. Clearly mention the partial output.

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