Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SIXTH SEMESTER BTECH. (ECE) DEGREE END SEMESTER EXAMINATION

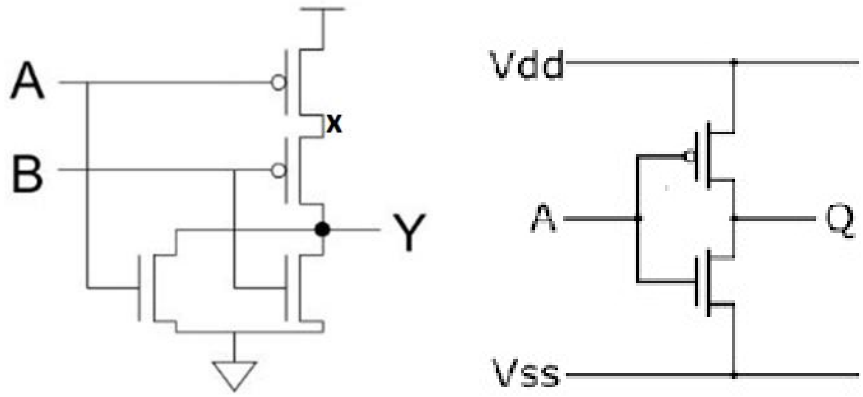
MAY 2023

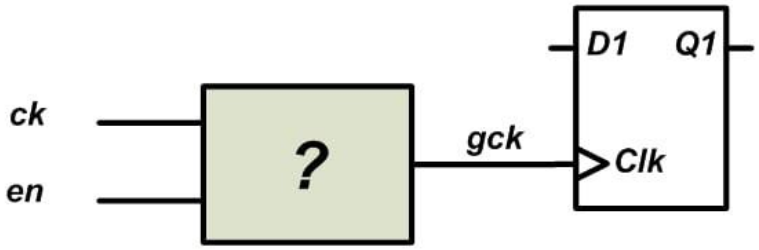
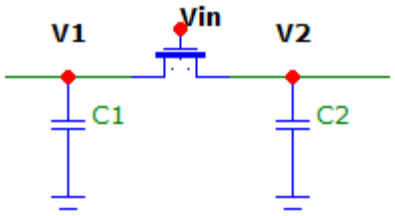
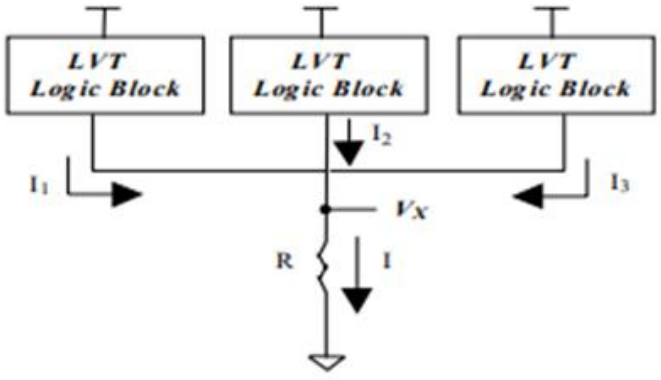
SUBJECT: LOW POWER VLSI (ECE -4063)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

Q. No.	Questions	M	CLO	A	BL
1A.	Orbit technology have fabricated CMOS based NOR2 and INV circuit as shown in Figure 1A. It has been observed that they have leakage current when devices are OFF. Following data have been obtained from the fab vendor: λ_d= 0.1 and sub-threshold swing S= 100 mV/decade, Vdd=1 V. (i) Calculate the Voltage Vx at node x, if VA=VB=1 in the NOR2 gate. (ii) Compare the leakage current of NOR2 gate and INV gate, when VA=1 in the INV gate.  (a) (b) **Figure 1A.**	4	**1**	**1**	**4**
1B.	Given the switching function F(A,B,C)= $\overline{(A+BC+B'C')}$, assume that all inputs toggle with a probability p1=0.5. Compute the activity factor α0->1 of the output.	3	**1**	**1**	**3**
1C.	A scheme for clock gating is shown in Figure 1C (i) Identify the gated block (ii) Write a Verilog code/pseudo code to simulate the gated D-FF.	3	**5**	**1,2**	**3**

	 **Figure 1C.**				
2A.	Illustrate the operation of 101+ 011 using Ripple carry adder using optimized TG cell. Further analysed the operation of one TG cell with example.	5	**4**	**1**	**4**
2B.	Compute the charge-sharing effects for the following cases assuming 130 nm technology parameters in Figure 2B. (i) C1=100 nF, C2= 20 fF, V1=0, V2=1.2 V. (ii) C1=20 nF, C2= 20 fF, V1=0, V2=1.2 V.  **Figure.2B**	3	**4**	**1**	**3**
2C.	Compare 4-T SRAM cell with resistive load and 6-T SRAM cell with PMOS load for low power applications with neat diagram.	2	**4**	**1**	**2**
3A.	Microsem technology has designed a power gated SOC where sleep transistor needs to be designed properly (Fig.3A). Engineer of Microsem have got following data from vendor for 180 nm: Vdd=1.8 V, velocity saturation index α=1.2, C_L= 1 pF, LVT=300 mV, HVT= 450 mV, $\mu nCox$=270 $\mu A/V^2$, I_1=350 μA, I_2= 1.8 (I_1/I_3), I_3=0.5 I_2. (i) Estimate the value of I_2 and I_3. (ii) Estimate τd and τd (sleep). (iii) If 8% degradation of performance is tolerated in presence of sleep transistor, calculate Vx. (iv) Design the width of the sleep transistor for proper performance.  **Figure 3A.**	5	**4**	**1**	**4**

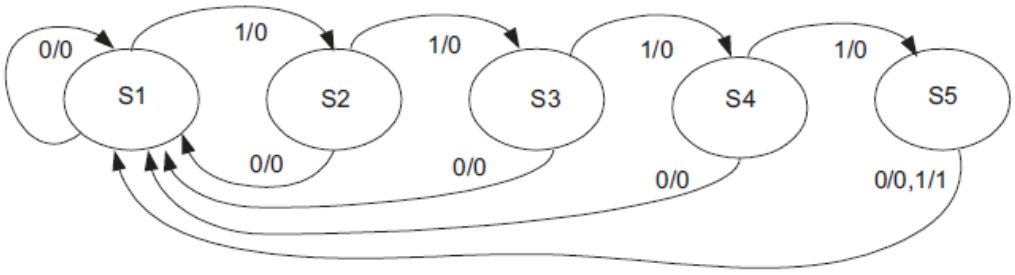
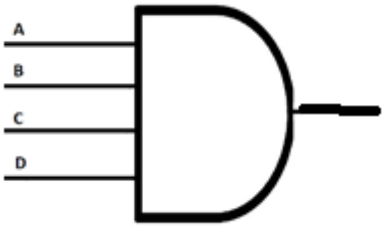
<table>
<tr><td>3B.</td><td>Illustrate with explanation different type of coarse grain structure for power gating.</td><td>3</td><td>4</td><td>1</td><td>3</td></tr>
<tr><td>3C.</td><td>Illustrate the implementation of F= $\overline{a+bc}$ using header type power switches.</td><td>2</td><td>4</td><td>1</td><td>3</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>4A.</td><td>TV tower is sending following set of serial data to the base station. It has been observed that a lot of power dissipation is taking place. Calculate the reduce no. of transitions, power dissipation, using SILENT coding technique on the data sent.
<table>
<tr><th>Name</th><th>T</th><th>T+1</th><th>T+2</th><th>T+3</th><th>T+4</th></tr>
<tr><td>D5</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>D4</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>D3</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>D2</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>D1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>D0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
</table></td><td>5</td><td>3</td><td>1</td><td>4</td></tr>
<tr><td>4B.</td><td>Consider the state-transition diagram of a sequence detector that produces “1” when five 1’s appears sequentially at the input (FIG.4B). In this case, the probability of all transitions p_{ij} is 0.5 and Weight W_{ij} is hamming distance between S_i and S_j. Calculate the objective function value for the Assignment 1- 000,111,001,110,101 and Assignment 2- 000,001,011,010,100.


Figure 4B.</td><td>3</td><td>3</td><td>1</td><td>4</td></tr>
<tr><td>4C.</td><td>8-bit data “00000000” needs to be send over the channel. Mr. X want to switch it to ‘ -1’ either in 2’s complement and signed magnitude form. Compare the two forms so that power dissipation can be reduced.</td><td>2</td><td>3</td><td>1</td><td>3</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>5A.</td><td>Implement F= AB using (i) complementary pass transistor logic (ii) NORA logic (iii) Cascode voltage switch logic (iv) Swing-Restored Pass-Transistor Logic.</td><td>5</td><td>3</td><td>1</td><td>3</td></tr>
<tr><td>5B.</td><td>Compare the double edge-triggered FF over single edge-triggered FF with neat circuit diagram. Illustrate data loading in both cases.</td><td>3</td><td>2</td><td>1,3</td><td>2</td></tr>
</table>

5C.	Given, Ca < Cd. Pin A has lowest switching frequency and pin D has highest switching frequency. Pin B and C have same properties. Illustrate the pin swapping on 4-input AND gate as shown in figure 5C to reduce the power dissipations.  	2	**2**	**1,3**	**3**